JW7715

Synchronous Rectifier Controller

Parameters Subject to Change Without Notice

DESCRIPTION

JW®7715 is a synchronous rectifier controller application on Flyback converters which combined with an external MOSFET can replace the high efficiency schottky diode. If V_{SW} is lower than -300mV, it turns on gate.

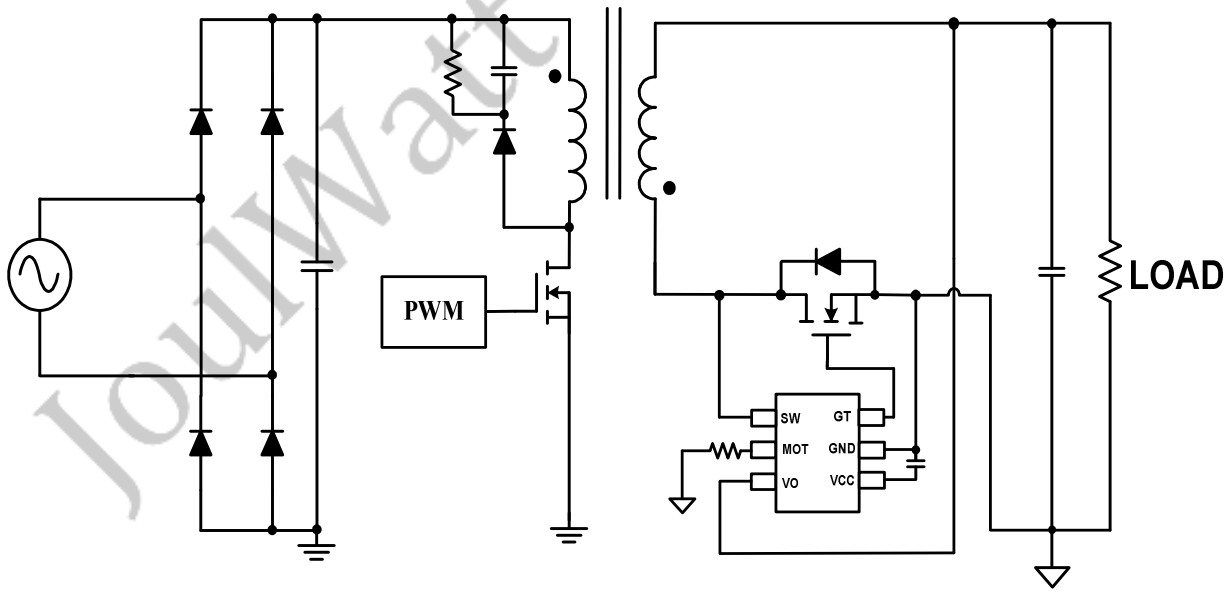
FEATURES

- Supports DCM ,Quasi-Resonant , CrCM and CCM Flyback converter
- Supports High-side and Low-side Rectification
- Vo directly supply VCC
- Low current consumption
- Under-voltage protection
- Fast driver capability

APPLICATIONS

- Flyback converters
- Adaptors

TYPICAL APPLICATION



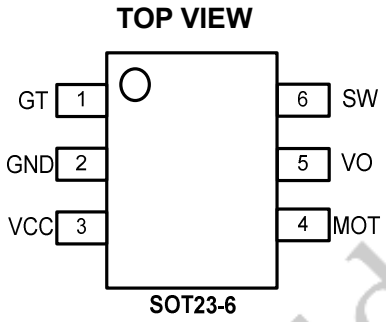
ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PACKAGE	TOP MARKING
JW7715SOTB#PBF	JW7715SOTB#TRPBF	SOT23-6	JWE3

Note：

JWXXXXPPPP#TRPBF
- Pb Free
- Tape and Reel（If "TR" is not shown, it means Tube）
- Package Code
- Part Number

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING[1)]

SW PIN 80V
VO PIN 30V
VCC, GT PIN.....5V
Maximum Power Dissipation[2)].....0.5W
Junction Temperature[3)].....150ºC
Lead Temperature 260ºC
Storage Temperature.....-65ºC to150ºC

RECOMMENDED OPERATING CONDITIONS

SW Pin.....4.7V to 75V
VO Pin.....4.7V to 20V
VCC, GT PIN.....4V to 6V
Operation Junction Temp. ..... -40ºC to 125ºC

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}
SOT23-6	220	130ºC/W

Note：

1) Exceeding these ratings may damage the device.

2) TA=25℃. The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$.

3) The JW7715 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

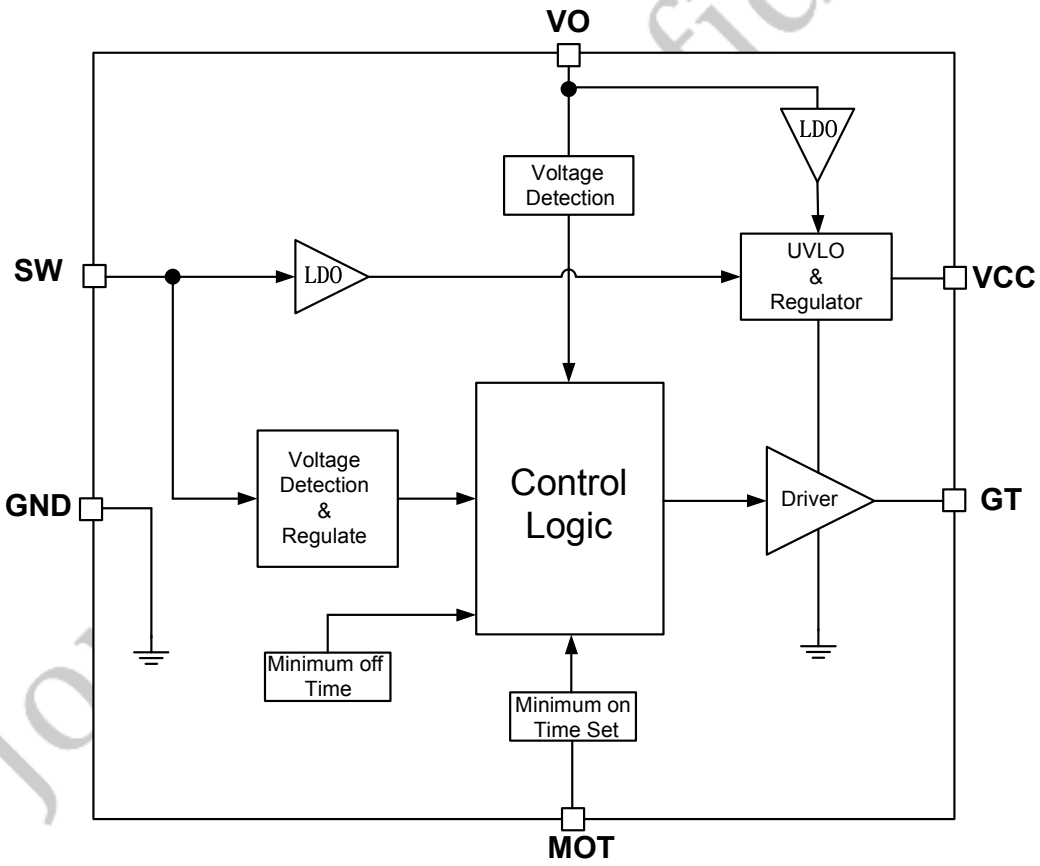
TA = 25ºC, unless otherwise stated

Item	Symbol	Condition	Min.	Typ.	Max.	Units
VCC Section						
VCC Voltage	V_{CC}	SW=40V, VCC=0.1uF		5.27		V
VCC Startup voltage	$V_{CC\_Startup}$		3.64	3.7	3.76	V
VCC UVLO	V_{CC_UVLO}		3.43	3.5	3.57	V
Operation Current (Switching)	I_{SW}	GT=5nF, Fsw=100KHz	4	6	8	mA
Operation Current (GT On)	I_{VCC}	GT=5nF,VCC=0.1uF		1		mA
Quiescent Current	I_q	VCC=4.5V, VCC=0.1uF	35	41	49	uA
Gate Section						
Gate Turn on Threshold	V_{MOS_ON}			-300		mV
Gate Turn off Threshold	V_{MOS_OFF}			-10		mV
Gate Turn off Threshold in MOT	$V_{MOS\_OFF\_MOT}$			50		mV
Gate Enable Threshold	$V_{MOS\_EN\_ON}$			4		V
Gate Turn on Voltage	V_{GT}	SW=40V, VCC=0.1uF	V_{CC}-1	V_{CC}		V
Gate Pull up current	I_{GU}	GT=1V	1.5	2	2.5	A
Gate Pull down current	I_{GD}	GT=5V	3.7	4.6	5.5	A
Gate Minimum on Time	T_{MIN_ON}	RMOT=100K		1.5		uS
		RMOT=0Ω		550		nS
Gate Minimum off Time	T_{MIN_OFF}			300		nS
Turn-on total delay	T_{DON}	R_{GATE}=0Ω, C_{LOAD}=5nF			50	nS
		R_{GATE}=0Ω, C_{LOAD}=10nF			70	
Turn-off total delay	T_{DOF}	R_{GATE}=0Ω, C_{LOAD}=5nF			10	nS
		R_{GATE}=0Ω, C_{LOAD}=10nF			20	
SW and Vo Section						
VCC Charge Current	I_{CV}	SW=40V, VCC=4V	50	55	60	mA
SW Control Voltage	V_{MOS_REG}			-60		mV
SW Control Voltage MAX	$V_{MOS\_REG\_MAX}$	Metal option-- remove		-120		mV
VO Enable Charge Voltage	V_{O_EN}	VCC=3V, SW=0V	4.6	4.7	4.8	V
VO Disable Charge Voltage	V_{O_DIS}	VCC=3V, SW=0V	4.4	4.5	4.6	V
VO Charge Current	I_{VO_CHG}	SW=0V, VCC=3，VO=5V	37	40	43	mA
Vo Short-circuit Detection Voltage	V_{O_SHORT}		1.8	2	2.2	V

PIN DESCRIPTION

Pin No.	Name	Description
1	GT	Drive the External NMOSFET.
2	GND	Ground.
3	VCC	Power supply. Bypass a Capacitor Between VCC and GND.
4	MOT	Set the minimum on-time, floating the pin means 300ns
5	VO	Output Voltage Sensing and Charging to VCC.
6	SW	External Power NMOSFET Drain Voltage Sensing. Charging to VCC.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Operation

JW7715 is a synchronous rectifier controller which combine with external MOSFET can replace the Schottky Barrier Diode to improve significantly the efficiency in flyback converters. It supports many operations, such as DCM, CrCM, Quasi-Resonant and CCM when application on flyback converters.

Startup

During the startup period, when the VCC is lower than startup voltage, the external NOSFET is turned off. The current flows though body diode before the VCC reaches to the startup voltage.

Under-Voltage Lockout (UVLO)

When the VCC is below UVLO threshold, the external MOSFET is turned off and never turned on before the VCC exceeds the startup voltage.

LDO Charging Logic

JW7715 have two inner LDO charging to VCC. When VO is lower than 4.65V, JW7715 can power itself through the internal LDO connected SW during the turn-off period which means primary MOSFET is turned on and SW is a positive voltage. A capacitor is needed between VCC and GND to store energy and supply to IC during the turn-on period.

The other inner LDO connected from VO to VCC, it charges to VCC when VO is higher than 4.65V.

Turn On Phase

When the synchronous MOEFET is conducting, current flows through the body diode of MOSFET, which generates a negative voltage V_{SW}. When V_{SW} is lower than V_{MOS_ON}, the synchronous MOSFET turns on after the turn on delay T_{DON}.

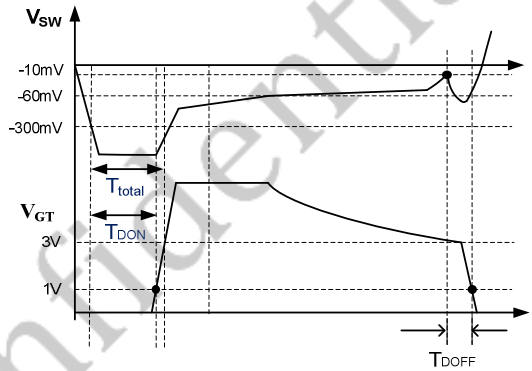


Figure-1 Turn on delay and turn off delay

Conducting Phase

The JW7715 has a special turn on logic in case of serious recover current which is cause by the gate error turn on when the magnetizing inductor and parasitic capacitor is resonant after conducting. The V_{SW} is regulated at -60mV the instant the synchronous MOSFET turn on. The synchronous MOSFET is fully on once the V_{SW} is high than -60mV.

The control circuit contains a minimum on time function. The V_{SW} voltage may have a ring when the synchronous MOSFET turns on, which is caused by parasitic inductor. So a minimum on time (MOT) is very valuable to avoid the MOSFET turn off threshold is trigger. There is not absolutely blanking during the minimum on time which means gate can be turned off if V_{SW} touches a positive threshold value,+50mV.

The V_{SW} decreases with the current follow through the MOSFET decreasing. When the V_{SW} is lower than -60mV, the gate keep its maximum voltage. The gate will be decreased and regulate the V_{SW} around -60mV, once the V_{SW} approaching -60mV.

Figure-2 shows synchronous rectification application on DCM mode.

Figure-3 shows synchronous rectification application on CCM mode.

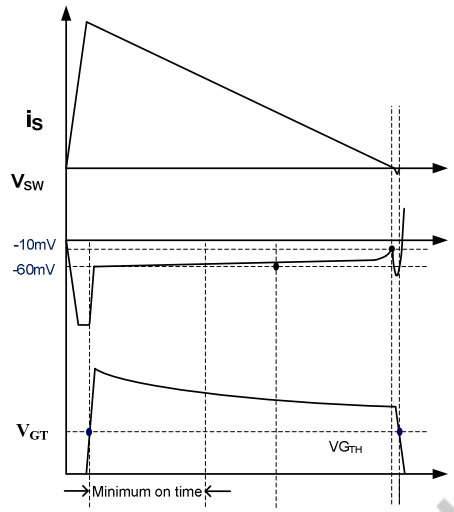


Figure-2 Conducting phase for DCM mode

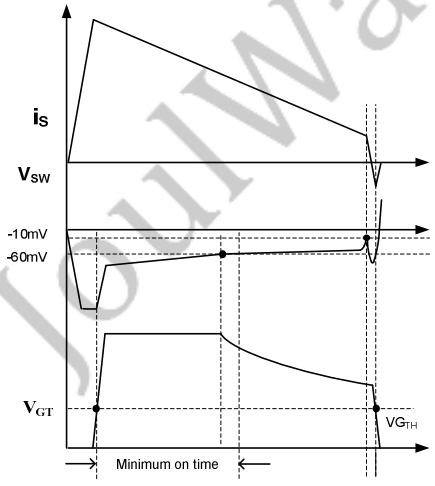


Figure-3 Conducting phase for CCM mode

Turn Off Phase

After synchronous MOSFET conducting, once the voltage of V_{SW} touches the MOSFET turn off threshold (-10mV), the gate is pulled down to low after the turn off delay T_{DOFF}. A 300nS blanking time is necessary to avoid error trigger.

Minimum on-time (MOT)

MOT stands for minimum on time of SR MOSFET or the maximum duty cycle of primary MOSFET, The MOT can be adjusted by a resistor placed on MOT pin. The relation between MOT and the resistor is as following, Shorting MOT to GND set MOT to maximum 2us, and floating MOT turns out to minimum 300ns.

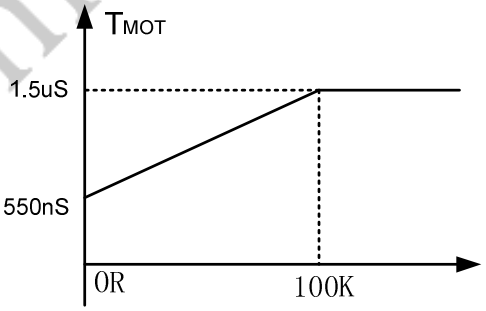


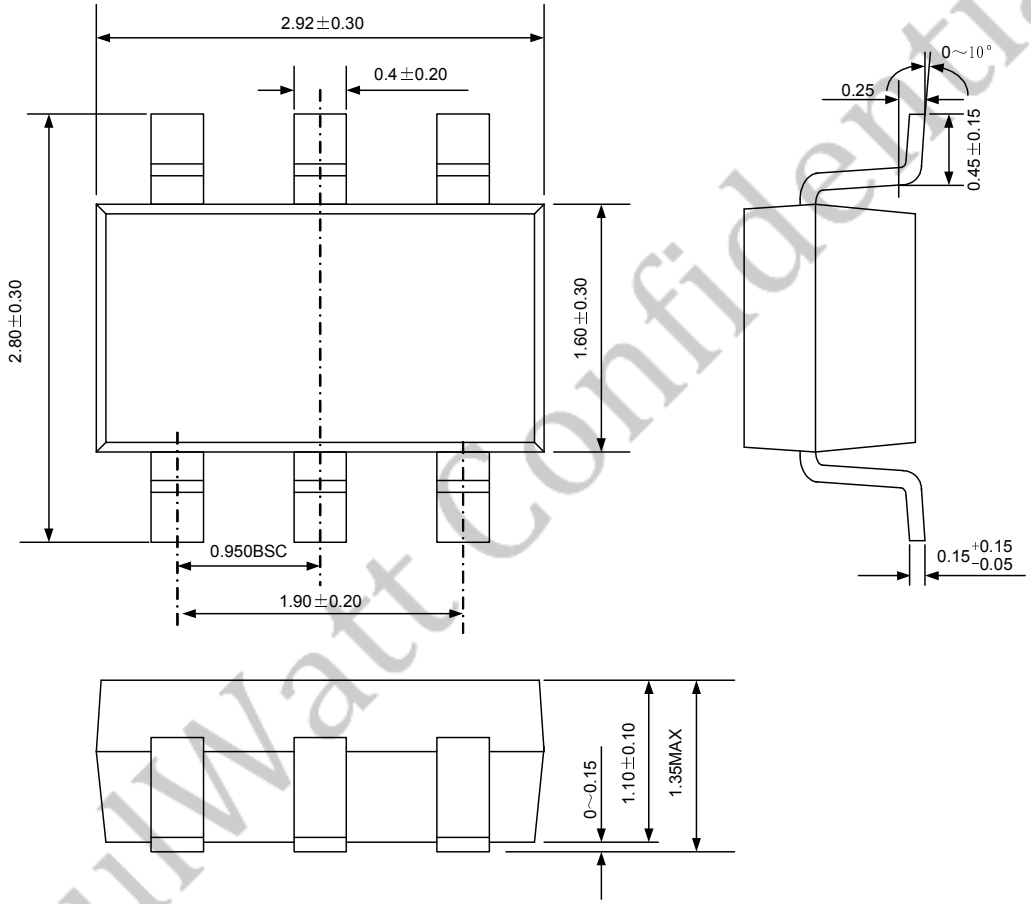
Figure-4 t_{MOT} v.s. R_{MOT}

Output Voltage Detection

The JW7715 has output voltage detection function via V_O pin. To avoid the gate error turn on when starting-up, the whole SR control logic is disabled when the V_O voltage is lower than 2V. VCC is charged from V_O pin when V_O is higher than 4.65V to save inner LDO power loss caused by charging from SW pin to VCC pin.

PACKAGE OUTLINE

SOT23-6 **UNIT:** mm



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