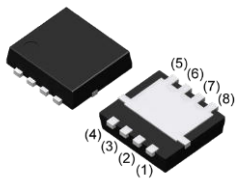
AD30P47D3

Datasheet

V_{DSS}	-30V
$R_{DS(on)}$(Max.)	8.5mΩ
I_D	±47A
P_D	38W

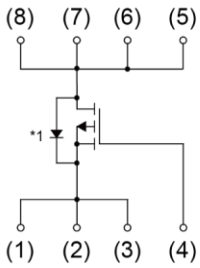
Outline

HSMT8



Inner circuit

(1) Source
(2) Source
(3) Source
(4) Gate
(5) Drain
(6) Drain
(7) Drain
(8) Drain
*1 Body Diode



Features

1)Low on - resistance.
2)High Power small mold Package (HSMT8).
3)Pb-free lead plating ; RoHS compliant.
4)Halogen Free.

Application

Switching

Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	330
	Tape width (mm)	12
	Basic ordering unit (pcs)	5000
	Taping code	D3
	Marking	AD30P47D3

Absolute maximum ratings (T_a = 25°C ,unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain - Source voltage		V_{DSS}	-30	V
Continuous drain current	T_c = 25°C	I	±47	A
	T_c= 100°C	I_D	±30	A
Pulsed drain current		I_D	±188	A
Gate - Source voltage		V_{GSS}	±25	V
Avalanche current, single pulse		I_A	-12	A
Avalanche energy, single pulse		E_A	81	mJ
Power dissipation		P T_c = 25°C	38	W
		P T_C= 25°C	3.5	W
Junction temperature		T_j	150	°C
Operating junction and storage temperature range		T_{stg}	-55 to +150	°C

Electrical characteristics (T_a = 25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V,V_{GS}=0V	--	--	-1	μA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=-30V,V_{GS}=0V	--	--	-100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±25V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=-250μA	-1.2	-1.8	-2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	V_{GS}=-10V, I_D=-20A	--	8.5	11	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ④	V_{GS}=-4.5V, I_D=-10A	--	15	20	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=-15V,V_{GS}=0V, f=1MHz	2820	3320	3820	pF
C_{oss}	Output Capacitance		335	395	455	pF
C_{rss}	Reverse Transfer Capacitance		210	245	280	pF
R_g	Gate Resistance	f=1MHz	--	2.3	--	Ω
Q_g (10V)	Total Gate Charge	V_{DS}=-15V,I_D=-10A, V_{GS}=-10V	--	39	--	nC
Q_g (4.5V)	Total Gate Charge		--	22.3	--	nC
Q_{gs}	Gate-Source Charge		--	7	--	nC
Q_{gd}	Gate-Drain Charge		--	11	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=-15V, I_D=-10A, R_G=6.8Ω, V_{GS}=-10V	--	15	--	ns
t_r	Turn-on Rise Time		--	33	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	67	--	ns
t_f	Turn-Off Fall Time		--	21	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=-20A,V_{GS}=0V	--	-0.89	-1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=-10A, V_{GS}=0V di/dt=-100A/μs	--	29	--	ns
Q_{rr}	Reverse Recovery Charge			144		nC

Thermal resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	35	°C/W

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by TJ max, starting TJ = 25°C, L = 0.5mH, RG = 25Ω, IAS = -18A, VGS =-10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

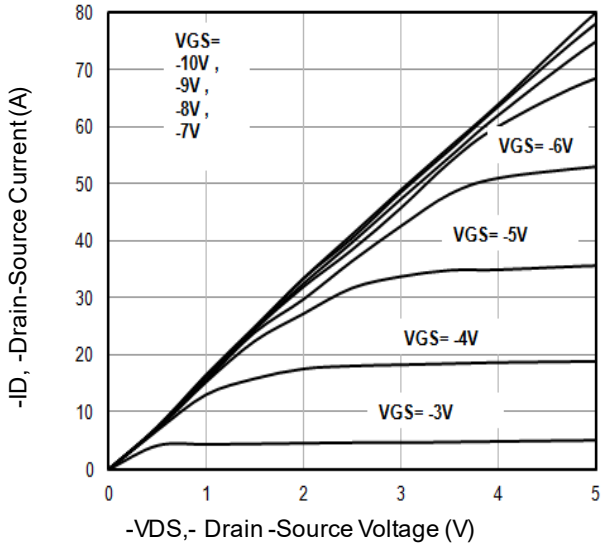


Fig1. Typical Output Characteristics

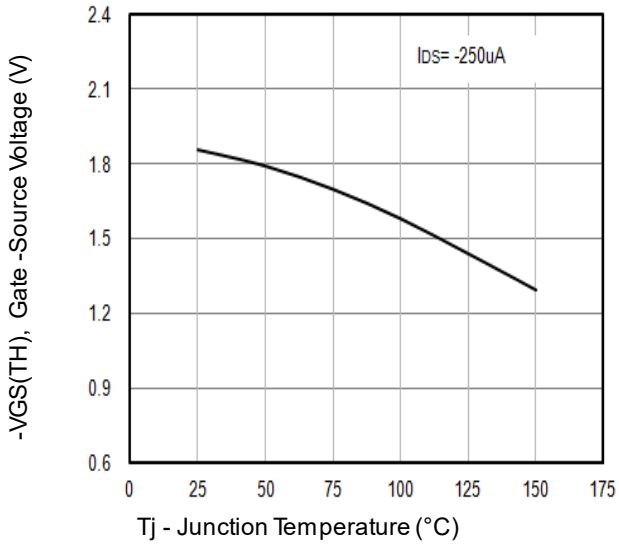


Fig2. $-V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

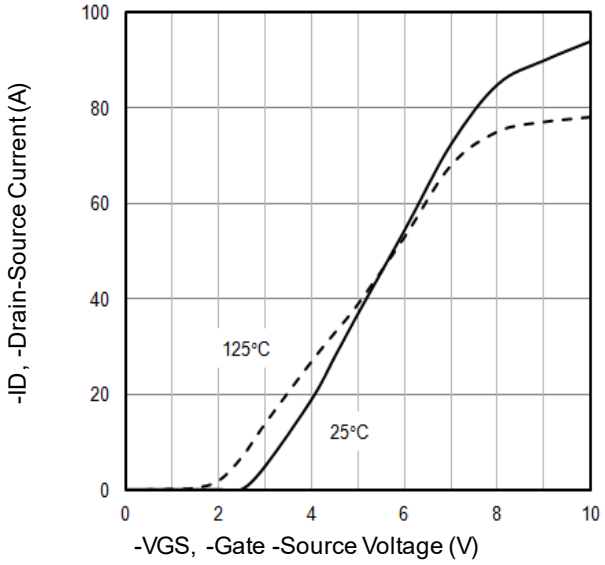


Fig3. Typical Transfer Characteristics

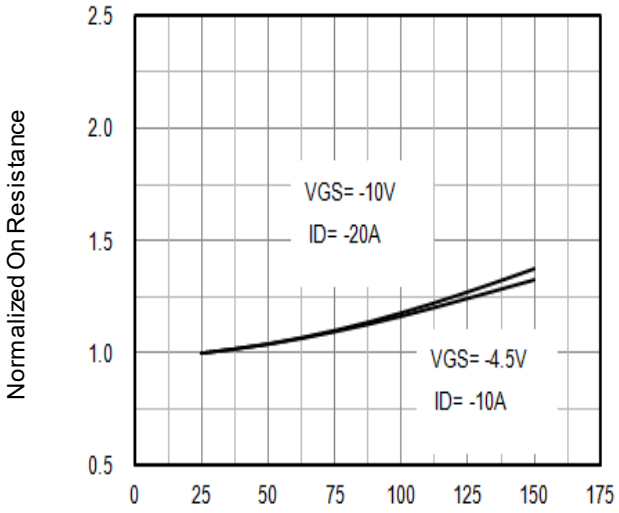


Fig4. Normalized On-Resistance Vs. Tj

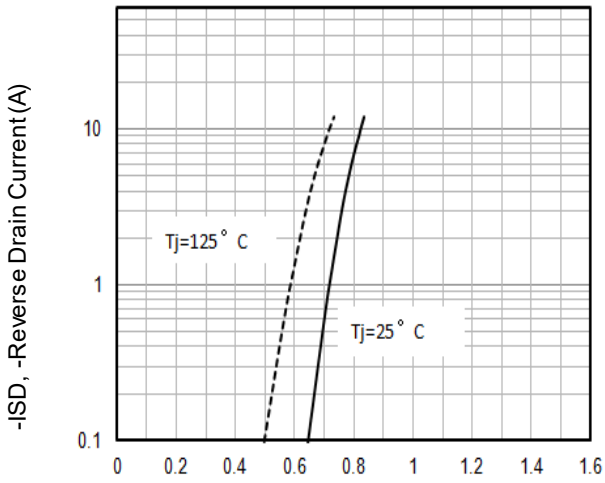


Fig5. Typical Source-Drain Diode Forward Voltage

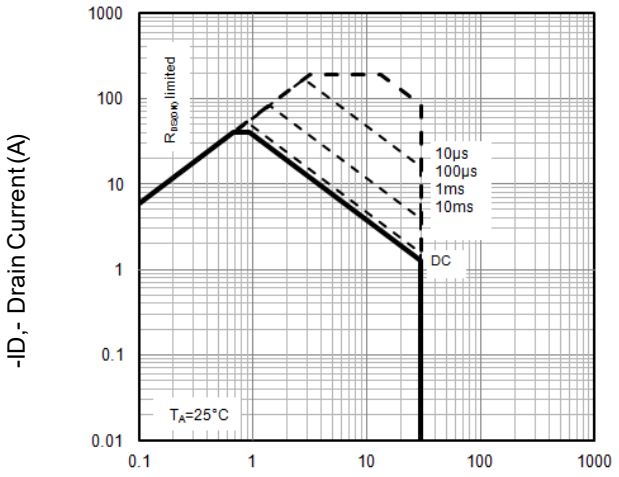


Fig6. Maximum Safe Operating Area

Electrical characteristic curves

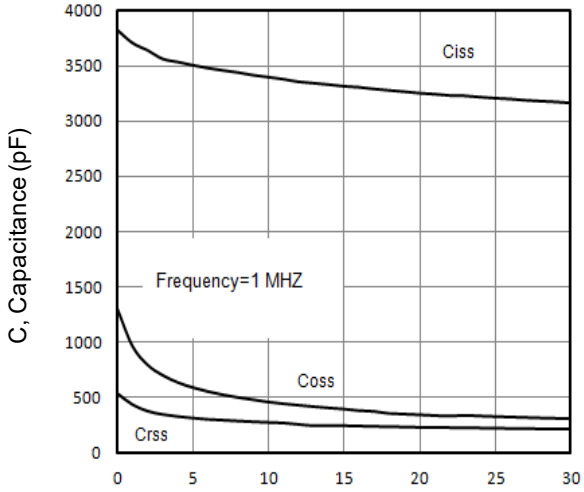


Fig7. Typical Capacitance Vs.Drain-Source Voltage

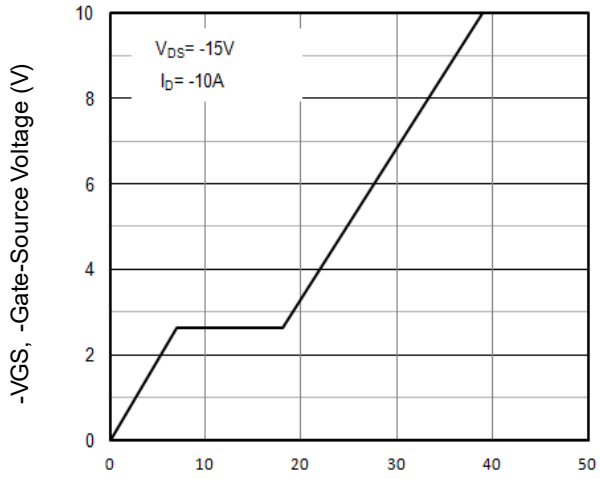


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

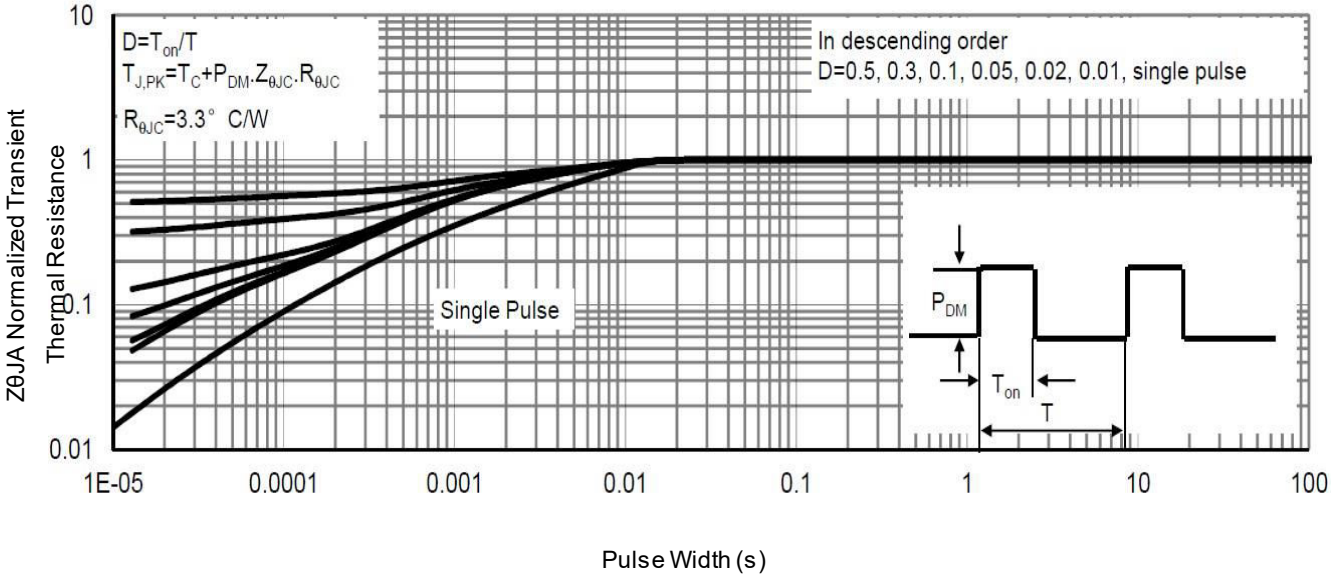


Fig9. Normalized Maximum Transient Thermal Impedance

Measurement circuits

Fig.1-1 Switching Time Measurement Circuit

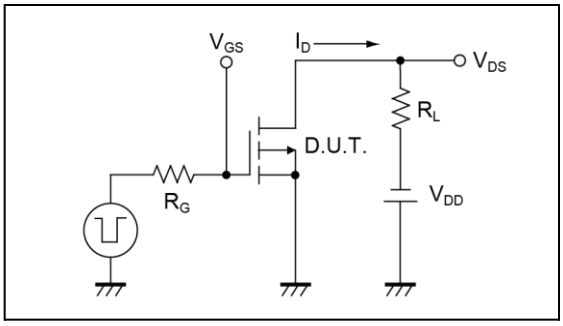


Fig.1-2 Switching Waveforms

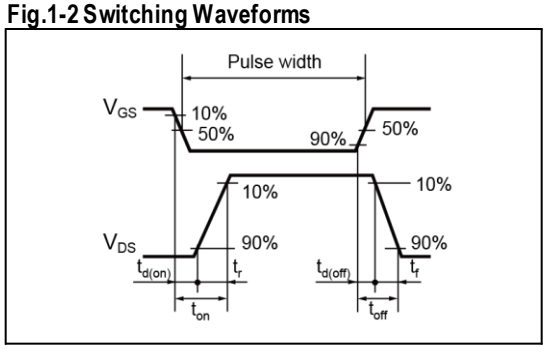


Fig.2-1 Gate Charge Measurement Circuit

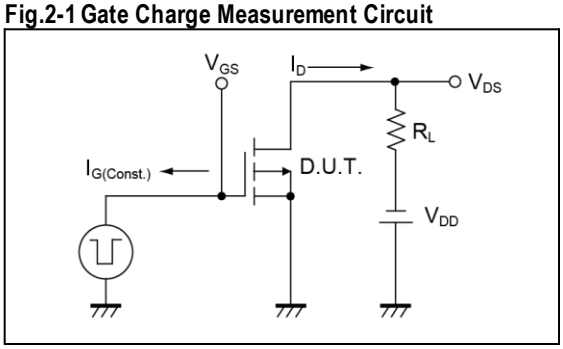


Fig.2-2 Gate Charge Waveform

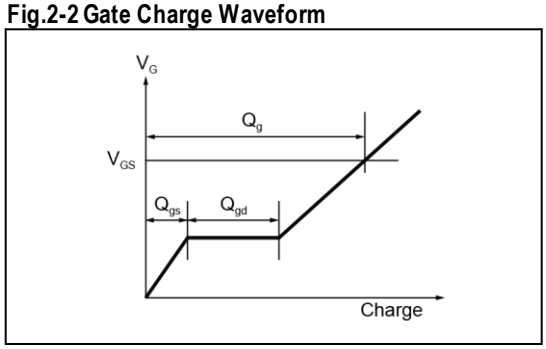


Fig.3-1 Avalanche Measurement Circuit

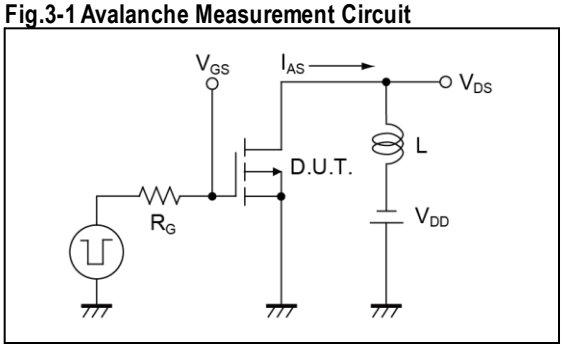
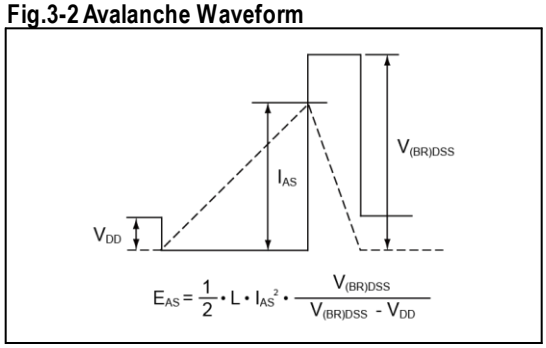


Fig.3-2 Avalanche Waveform



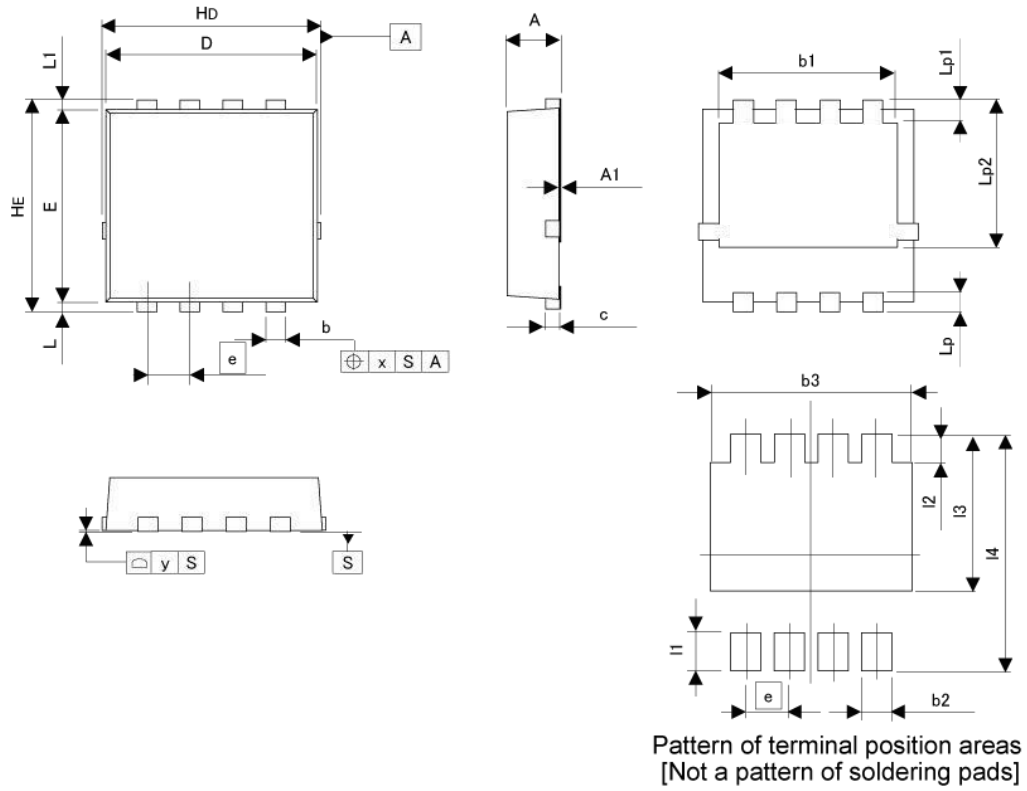
Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Dimensions

HSMT8

(3.3x3.3)



Pattern of terminal position areas
[Not a pattern of soldering pads]

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
A1	0.00	0.05	0.000	0.002
b	0.27	0.37	0.011	0.015
b1	2.50	2.70	0.098	0.106
c	0.10	0.30	0.004	0.012
D	3.10	3.30	0.122	0.130
E	2.90	3.10	0.114	0.122
e	0.65		0.026	
HD	3.20	3.40	0.126	0.134
HE	3.20	3.40	0.126	0.134
L	0.07	0.25	0.003	0.010
L1	0.07	0.25	0.003	0.010
Lp	0.20	0.40	0.008	0.016
Lp1	0.25	0.45	0.010	0.018
Lp2	2.20	2.40	0.087	0.094
x	-	0.10	-	0.004
y	-	0.10	-	0.004

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b2	-	0.47	-	0.019
b3	-	2.70	-	0.106
l1	-	0.50	-	0.020
l2	-	0.55	-	0.022
l3	-	2.40	-	0.094
l4	-	3.40	-	0.134

Dimension in mm/inches