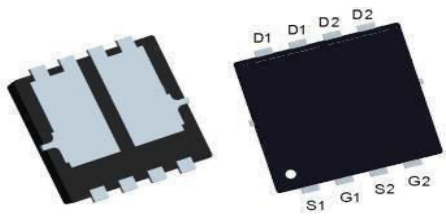
AD40K20D3

Datasheet

Symbol	Nch+Nch
V_{DSS}	40V
*R*DS(on),max@ *V*GS=10V	14mΩ
*R*DS(on),max@ *V*GS=4.5V	18.5mΩ
I_D	20A

Outline

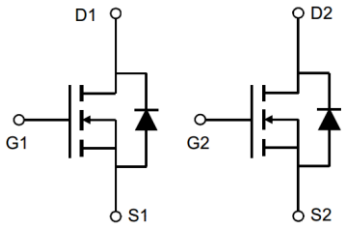
PDFN3333



Features

1)Low on - resistance
2)Pb-free lead plating ; RoHS compliant
3)Halogen Free

Inner circuit



Application

Switching

Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	180
	Tape width (mm)	8.0
	Basic ordering unit (pcs)	5000
	Taping code	TB
	Marking	AD40K20D3

Absolute maximum ratings (T_a = 25°C ,unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain - Source voltage		V_{DSS}	40	V
Continuous drain current	T_c = 25°C	I_D	20	A
	T_c= 100°C	I_D	14	A
Pulsed drain current		I_{DP}	90	A
Gate - Source voltage		V_{GSS}	±20	V
Avalanche current, single pulse		I_{AS}	22	A
Avalanche energy, single pulse		E_{AS}	70	mJ
Power dissipation		P_D	21	W
Junction temperature		T_j	150	°C
Operating junction and storage temperature range		T_{stg}	-55 to +150	°C

Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	R_{thJA}	-	-	53.4	°C/W

Electrical characteristics (T_a = 25°C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	40	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}$ / ΔT_j	I_D = 250uA referenced to 25°C	-	0.023	-	mV/°C
Zero gate voltage drain current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	-	-	1	μA
Gate - Source leakage current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250uA	1.0	1.5	2.5	V
Gate threshold voltage temperature coefficient	$\Delta V_{GS(th)}$ / ΔT_j	I_D = 250uA referenced to 25°C	-	-5.08	-	mV/°C
Static drain - source on - state resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	-	11	14	mΩ
		V_{GS} = 4.5V, I_D = 10A	-	14.3	18.5	
Gate resistance	R_G	f=1MHz, open drain	-	1.8	-	Ω
Forward Transfer Admittance	$\|Y_{fs}\|$	V_{DS} = 5V, I_D = 12A	-	24.4	-	S

Note :

1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3.The EAS data show s Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=22A

4.The power dissipation is limited by 175°C junction temperature

5.The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

Electrical characteristics (T_a = 25°C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 20V	-	750	-	pF
Output capacitance	C_{oss}	f = 1MHz	-	150	-	
Reverse transfer capacitance	C_{rss}		-	80	-	
Turn - on delay time	$t_{d(on)}$	V_{DD} ≒ 20V, V_{GS} = 10V	-	6	-	ns
Rise time	T_r	I_D = 20A R_G = 3Ω	-	17.5	-	
Turn - off delay time	$t_{d(off)}$	R_L = 1.5Ω	-	31	-	
Fall time	T_f		-	17	-	

Parameter	Symbol	Conditions		Values			Unit
				Min.	Typ.	Max.	
Total gate charge	Q_g	V_{DD} ≒ 20V I_D = 20A	V_{GS} = 10V	-	24.1	-	nC
			V_{GS} = 4.5V	-	15	-	
Gate - Source charge	Q_{gs}			-	3	-	
Gate - Drain charge	Q_{gd}			-	2.5	-	

Body diode electrical characteristics (Source-Drain) (T_a = 25°C)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous forward current	I_S	T_a = 25°C	-	-	35	A
Pulse forward current	I_{SP}		-	-	75	A
Forward voltage	V_{SD}	V_{GS} = 0V, Is = 1.67A	-	-	1.2	V
Reverse recovery time	T_{rr}	Is = 15A, V_{GS}=0V di/dt = 100A/μs	-	29	-	ns
Reverse recovery charge	Q_{rr}		-	26	-	nC

Electrical characteristic curves

Fig.1 Power Dissipation Derating Curve

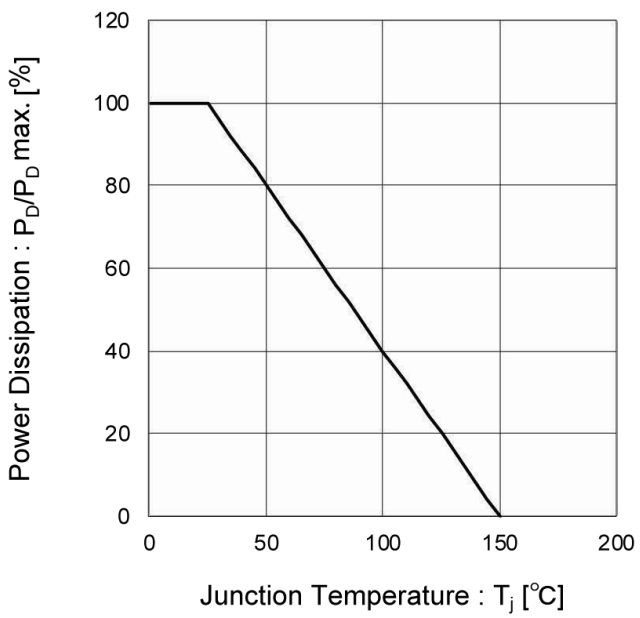
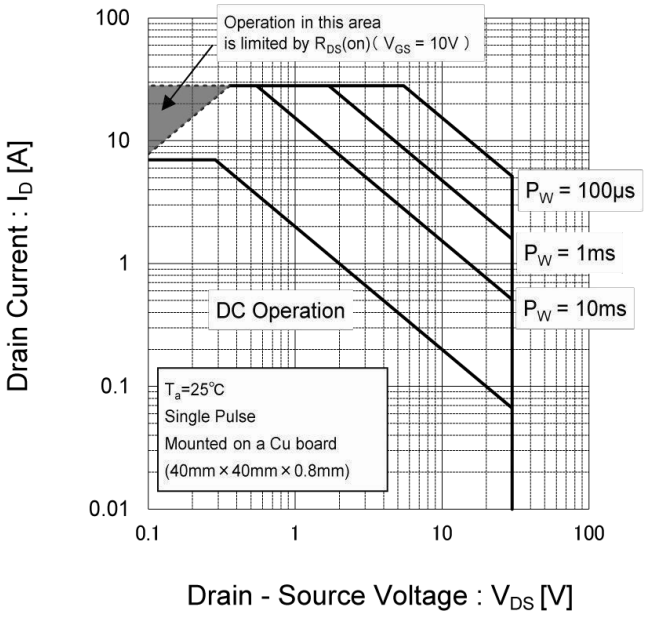


Fig.2 Maximum Safe Operating Area



Electrical characteristic curves

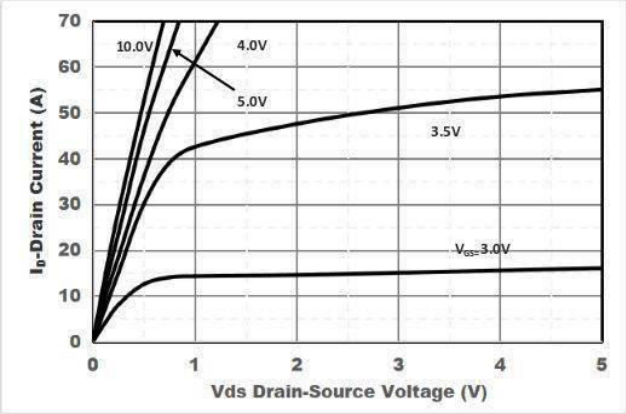


Figure1. Output Characteristics

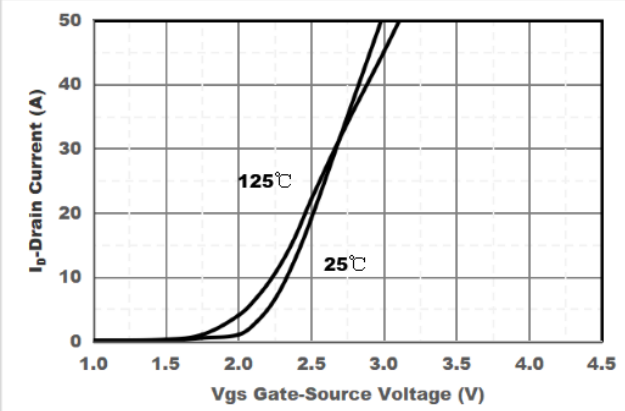


Figure2. Transfer Characteristics

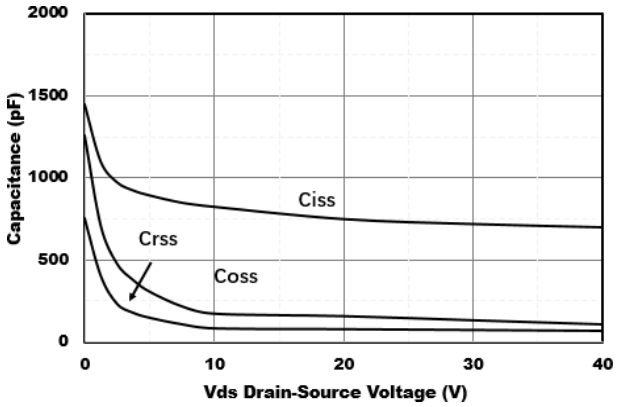


Figure3. Capacitance Characteristics

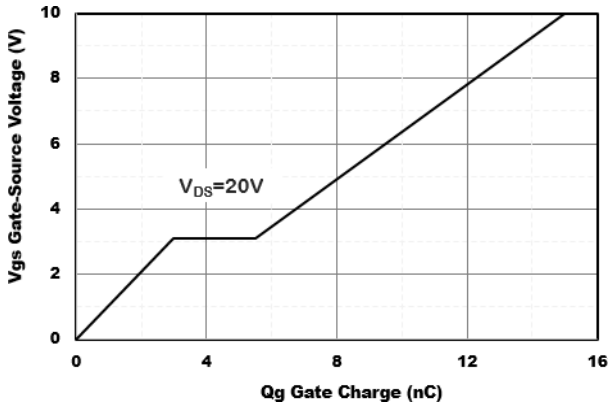


Figure4. Gate Charge

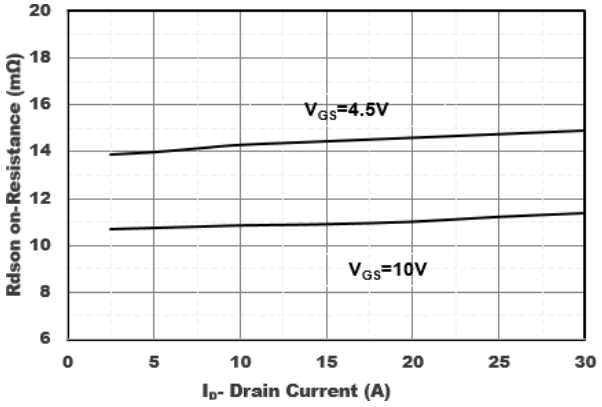


Figure5. Drain-Source on Resistance

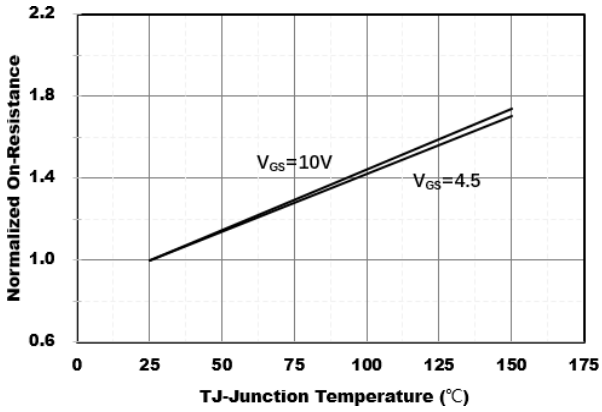


Figure6. Drain-Source on Resistance

Measurement circuits

Fig.1-1 Switching Time Measurement Circuit

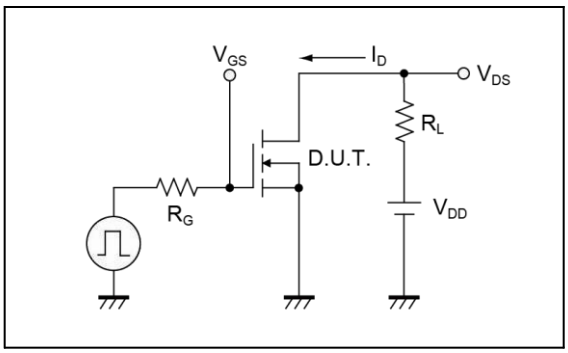


Fig.1-2 Switching Waveforms

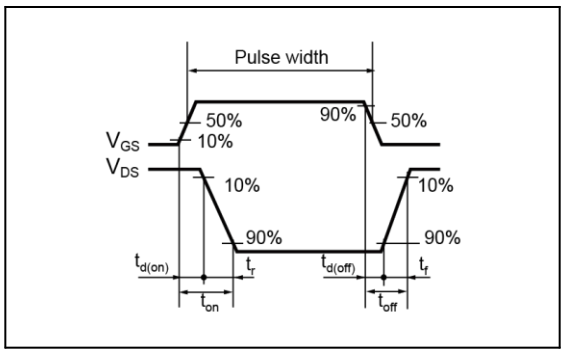


Fig.2-1 Gate Charge Measurement Circuit

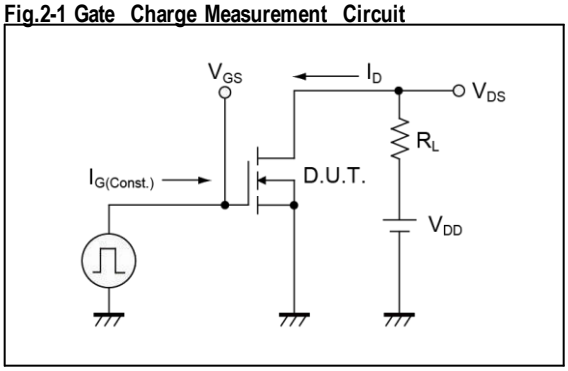


Fig.2-2 Gate Charge Waveform

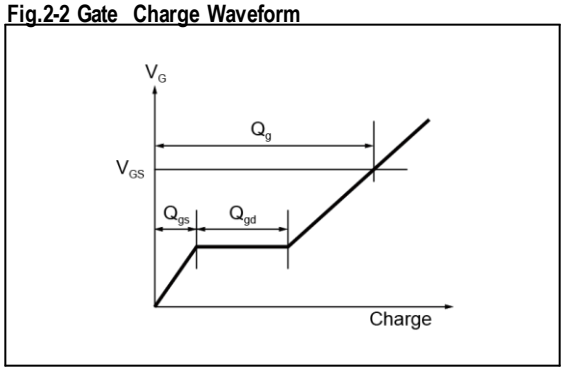


Fig.3-1 Avalanche Measurement Circuit

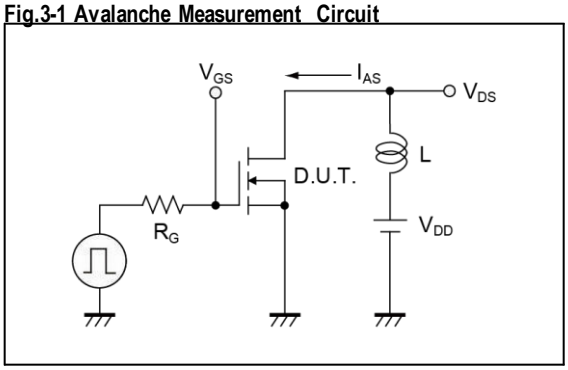
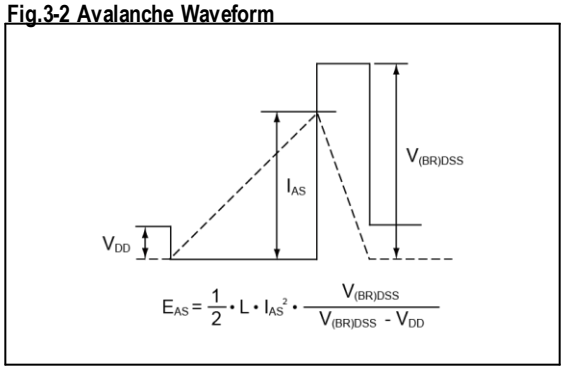


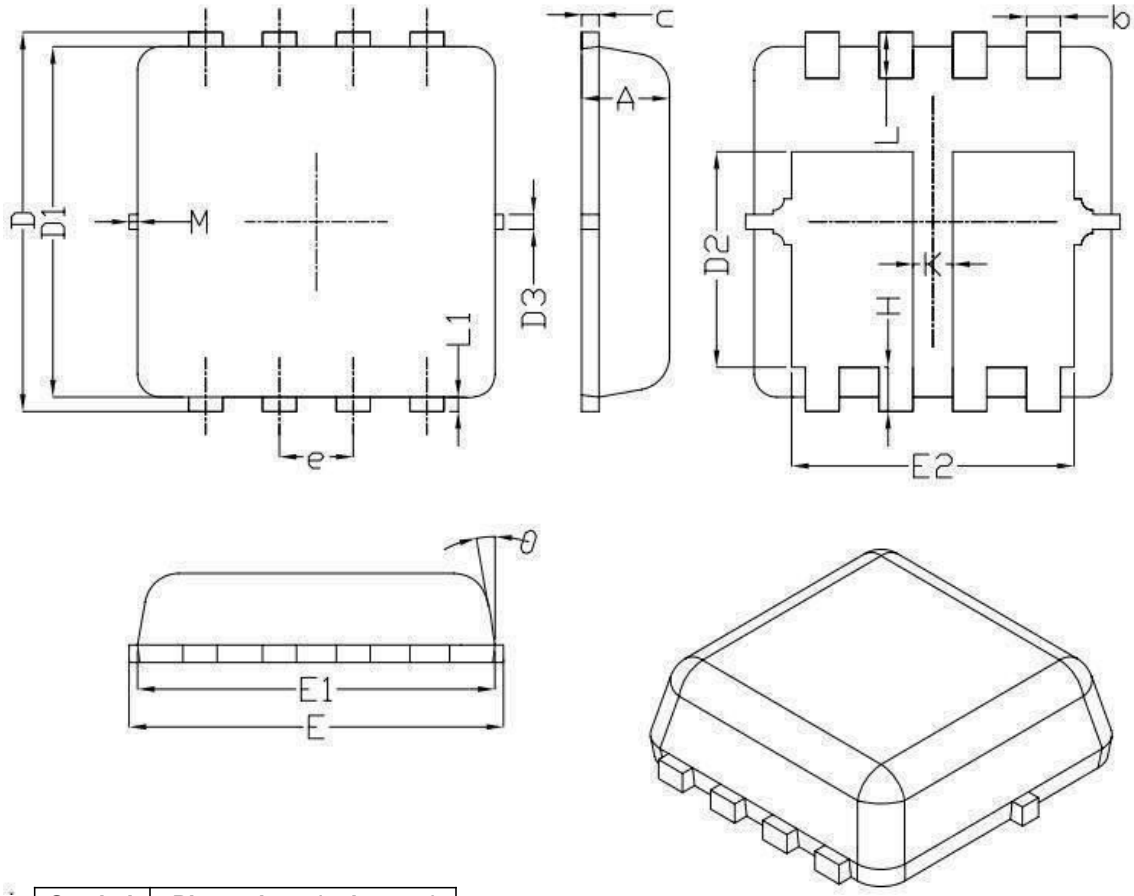
Fig.3-2 Avalanche Waveform



Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Dimensions



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			