

Symbol	Nch+Nch
V_{DSS}	30V
R_{D(on)},max@ V_{GS}=10V	12mΩ
R_{D(on)},max@ V_{GS}=4.5V	16mΩ
I_D	35A

Features

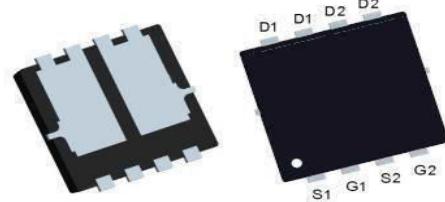
- 1) Low on - resistance
- 2) Pb-free lead plating ; RoHS compliant
- 3) Halogen Free

Application

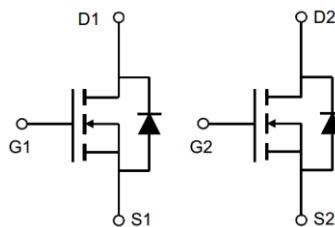
Switching

Outline

PDFN3333



Inner circuit



Packaging specifications

Type	Packing	Embossed Tape
Reel size (mm)	180	
Tape width (mm)	8.0	
Basic ordering unit (pcs)	5000	
Taping code	TB	
Marking	AD30K35D3	

Absolute maximum ratings (T_a = 25°C ,unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain - Source voltage	V _{DSS}	30	V
Continuous drain current	T _c = 25°C	I _D	A
	T _a = 25°C	I _D	9.5
Pulsed drain current	I _{DP}	75	A
Gate - Source voltage	V _{GSS}	±20	V
Avalanche current, single pulse	I _{AS}	22	A
Avalanche energy, single pulse	E _{AS}	22	mJ
Power dissipation	P _D	26	W
Junction temperature	T _j	150	°C
Operating junction and storage temperature range	T _{stg}	-55 to +150	°C

Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	R_{thJA}	-	-	75	°C/W

Electrical characteristics ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30	-	-	V
Breakdown voltage temperature coefficient	$\Delta V_{(BR)DSS}$ ΔT_j	$I_D = 250\mu\text{A}$ referenced to 25°C	-	0.023	-	mV/°C
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
Gate - Source leakage current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	-	2.5	V
Gate threshold voltage temperature coefficient	$\Delta V_{GS(th)}$ ΔT_j	$I_D = 250\mu\text{A}$ referenced to 25°C	-	-5.08	-	mV/°C
Static drain - source on - state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 15\text{A}$	-		12	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	-		16	
Gate resistance	R_G	f=1MHz, open drain	-	1.8	-	Ω
Forward Transfer Admittance	$ Y_{fs} $	$V_{DS} = 5\text{V}, I_D = 12\text{A}$	-	24.4	-	S

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$
- 3.The EAS data show s Max. rating . The test condition is $VDD=25\text{V}, VGS=10\text{V}, L=0.1\text{mH}, IAS=22\text{A}$
- 4.The power dissipation is limited by 175°C junction temperature
- 5.The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.

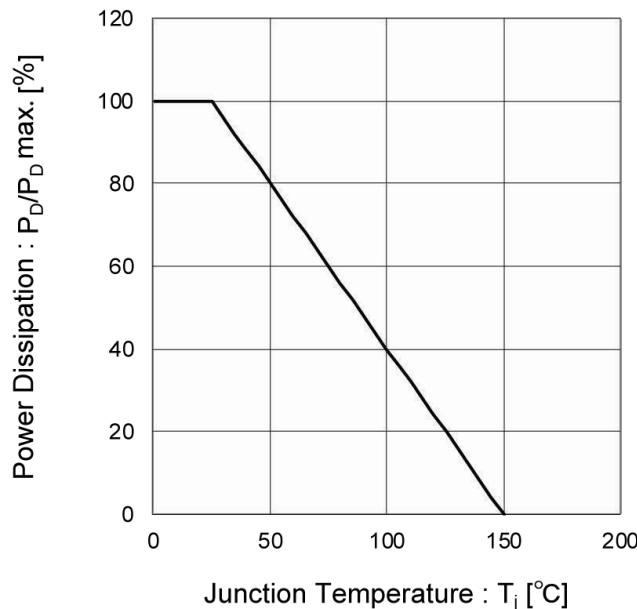
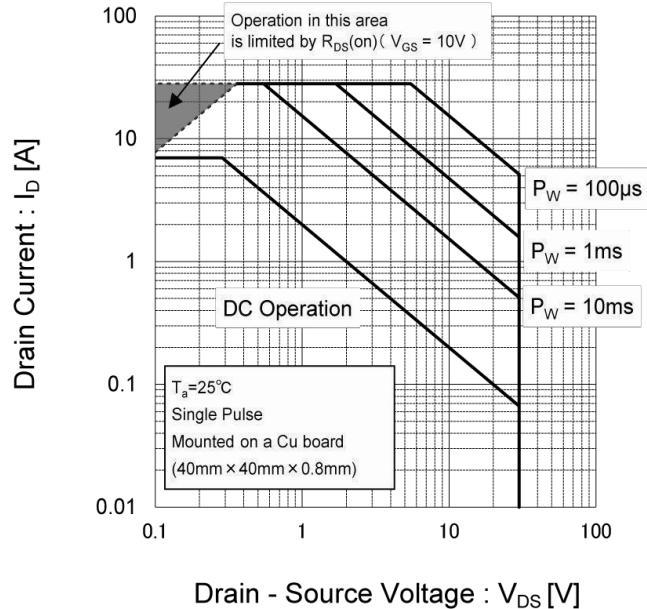
Electrical characteristics ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	$V_{GS} = 0\text{V}$ $V_{DS} = 15\text{V}$ $f = 1\text{MHz}$	-	896	-	pF
Output capacitance	C_{oss}		-	126	-	
Reverse transfer capacitance	C_{rss}		-	108	-	
Turn - on delay time	$t_{d(on)}$	$V_{DD} = 15\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 20\text{A}$ $R_G = 1.5\Omega$	-	6.4	-	ns
Rise time	T_r		-	39	-	
Turn - off delay time	$t_{d(off)}$		-	21	-	
Fall time	T_f		-	4.7	-	

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Total gate charge	Q_g	$V_{DD} = 15\text{V}$ $I_D = 12\text{A}$	-	14.1	-	nC
Gate - Source charge	Q_{gs}		-	9.82	-	
Gate - Drain charge	$Q_{g'd}$		-	2.24	-	
			-	5.54	-	

Body diode electrical characteristics (Source-Drain) ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous forward current	I_s	$T_a = 25^\circ\text{C}$	-	-	35	A
Pulse forward current	I_{sp}		-	-	75	
Forward voltage	V_{SD}	$V_{GS} = 0\text{V}$, $I_s = 1.67\text{A}$		-	1	V

Electrical characteristic curves**Fig.1 Power Dissipation Derating Curve****Fig.2 Maximum Safe Operating Area**

Electrical characteristic curves

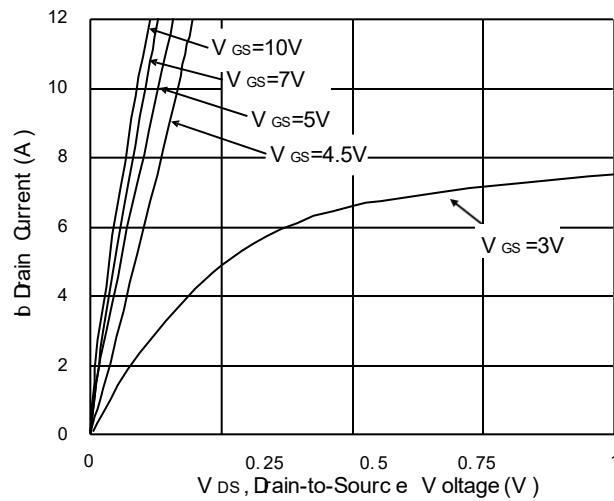


Fig.3 Typical Output Characteristics

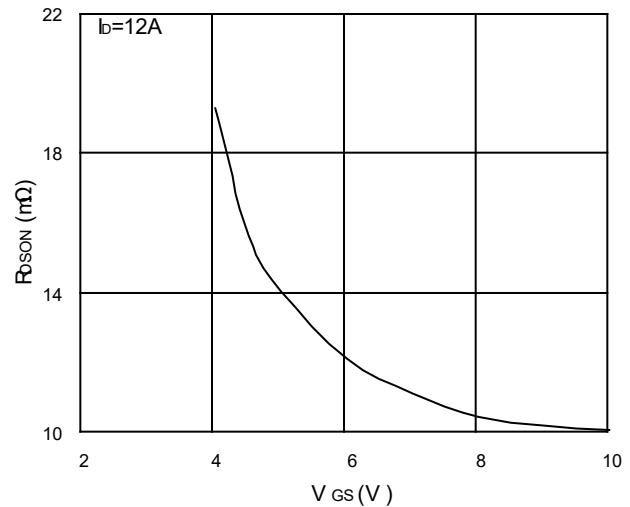


Fig.4 On-Resistance vs. G-S Voltage

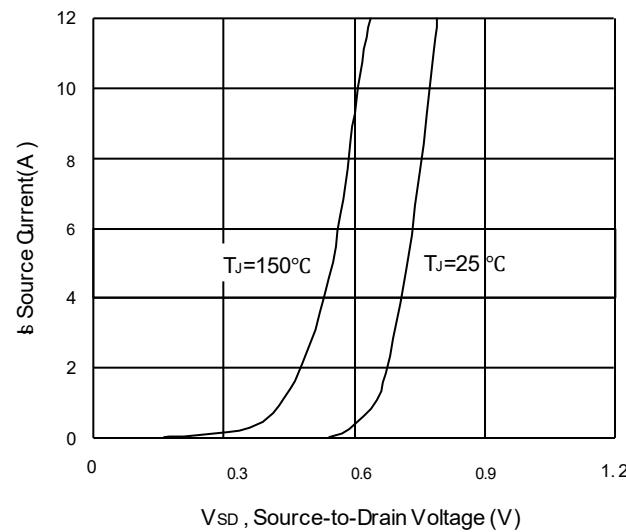


Fig.5 Forward Characteristics of Reverse

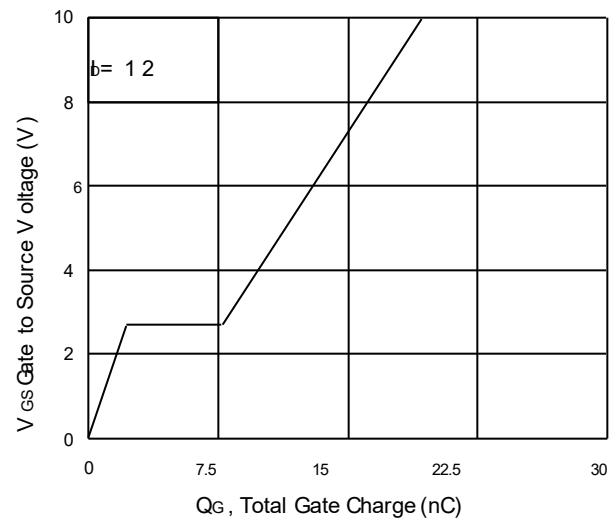


Fig.6 Gate-charge Characteristics

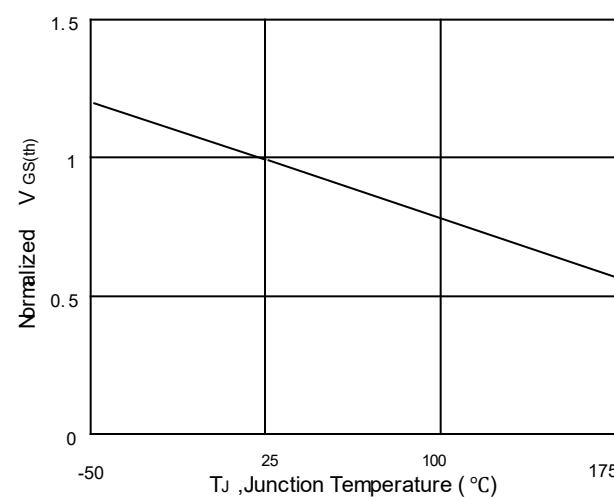


Fig.7 Normalized $V_{GS(th)}$ vs. T_J

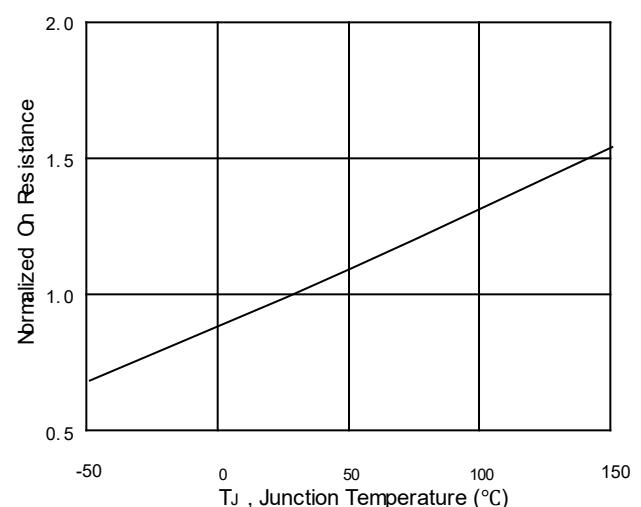


Fig.8 Normalized $R_{DS(on)}$ vs. T_J

Electrical characteristic curves

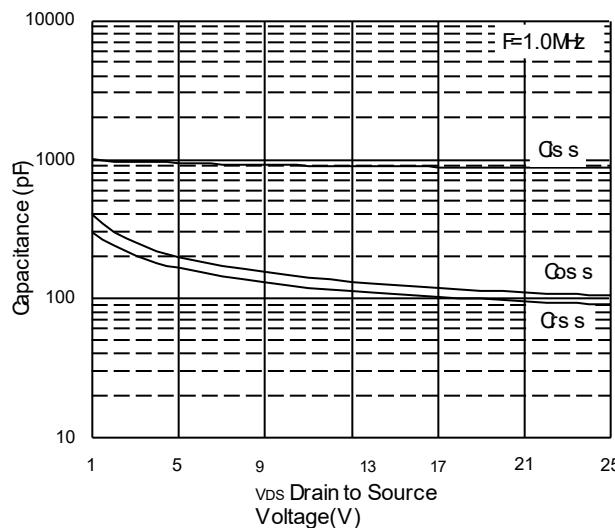


Fig.9 Capacitance

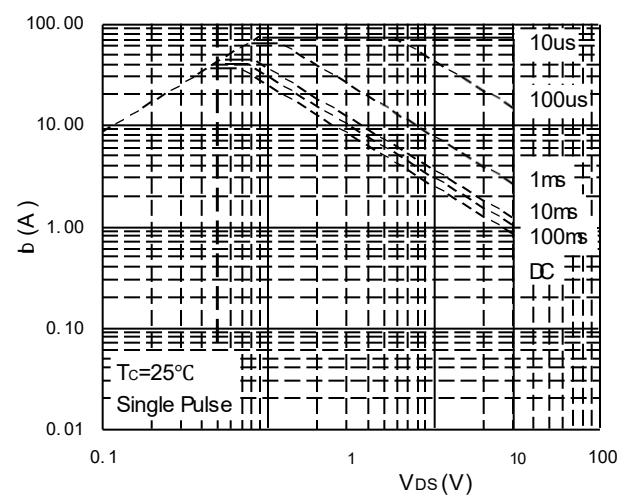


Fig.10 Safe Operating Area

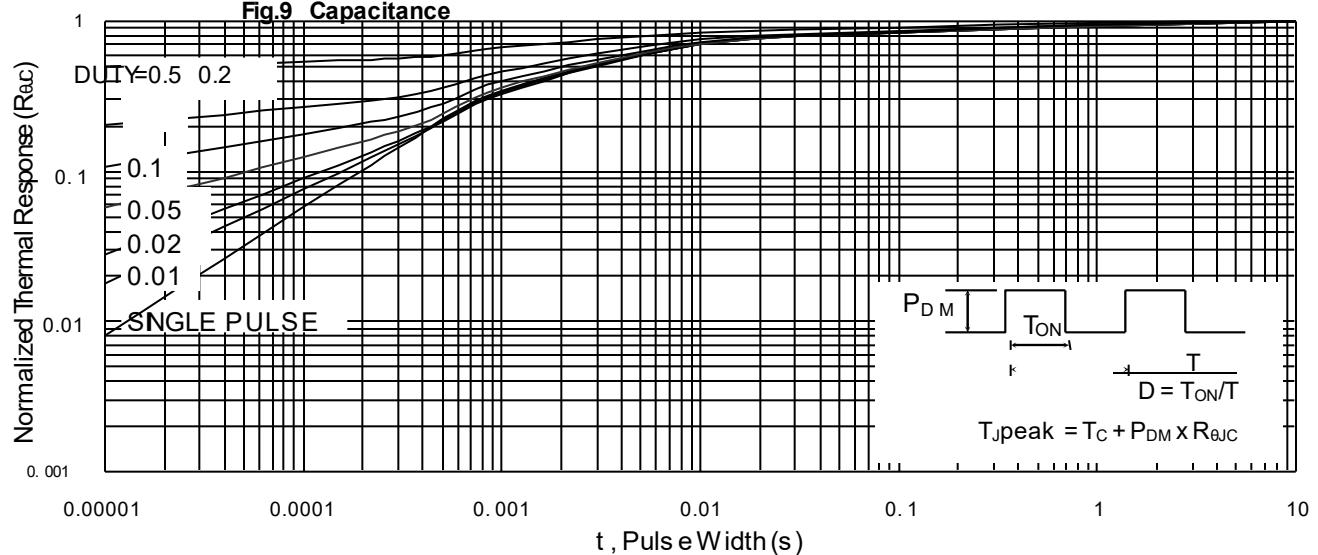


Fig.11 Normalized Maximum Transient Thermal Impedance

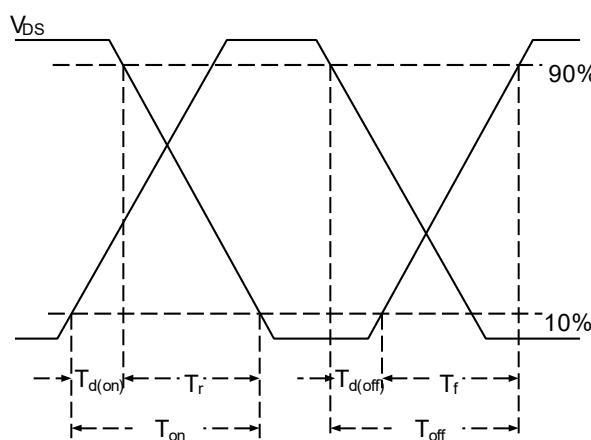


Fig.12 Switching Time Waveform

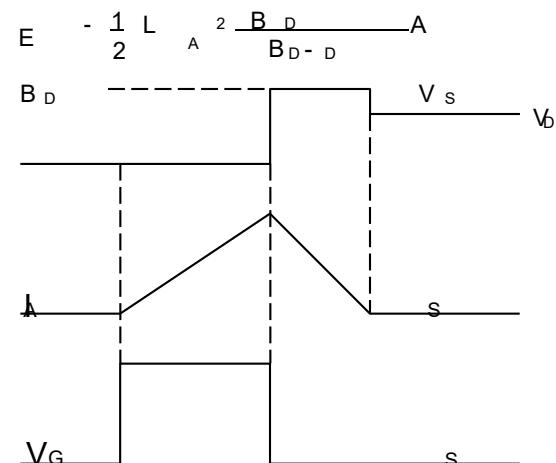


Fig.13 Unclamped Inductive Waveform

Measurement circuits

Fig.1-1 Switching Time Measurement Circuit

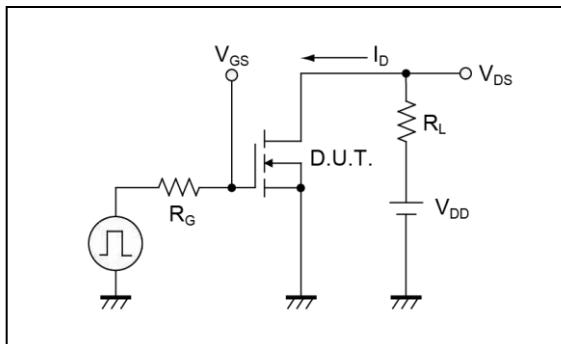


Fig.1-2 Switching Waveforms

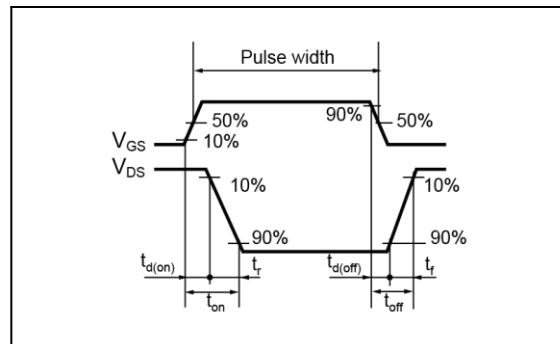


Fig.2-1 Gate Charge Measurement Circuit

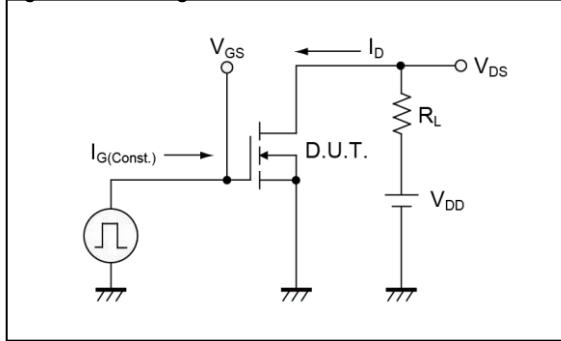


Fig.2-2 Gate Charge Waveform

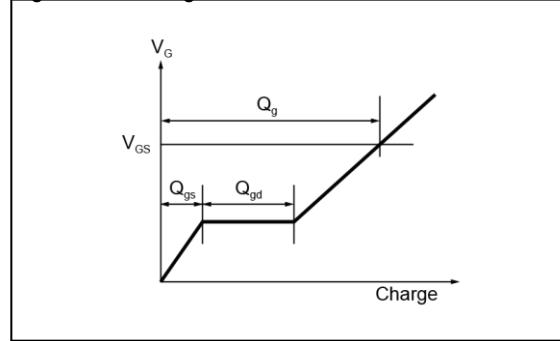


Fig.3-1 Avalanche Measurement Circuit

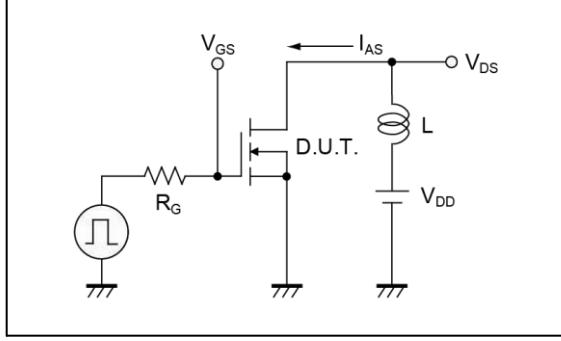
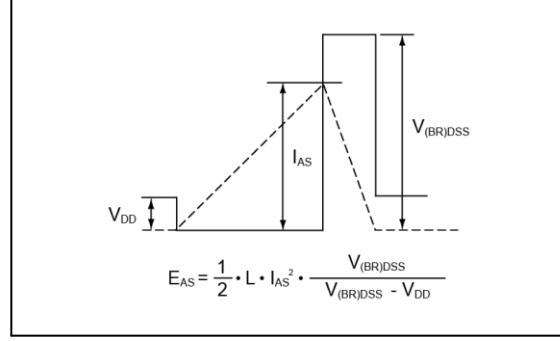


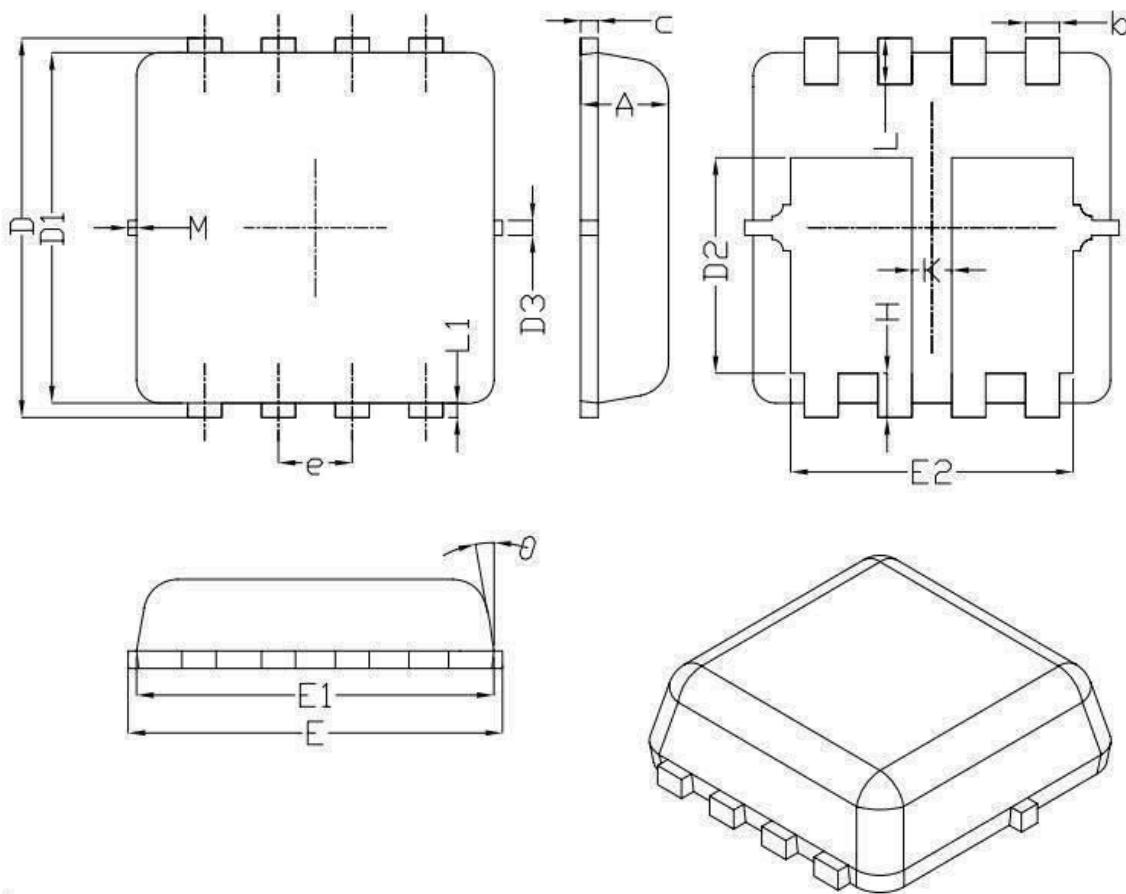
Fig.3-2 Avalanche Waveform



Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Dimensions



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			