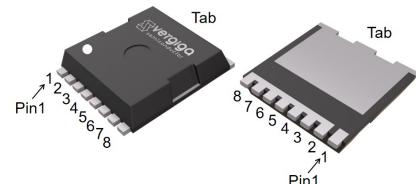


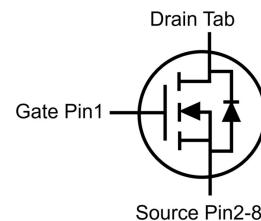
Features

- Enhancement mode
- Very Low on-resistance $R_{DS(on)}$
- VitoMOS® II Technology
- 100% Avalanche test

V_{DS}	80	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	2.4	$\text{m}\Omega$
I_D	240	A

TOLL

Halogen-Free

Part ID	Package Type	Marking	Packing
VSK003N08HS-G	TOLL	003N08H	2000PCS/Reel



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V(BR)DSS$	Drain-Source breakdown voltage	80	V
V_{GS}	Gate-Source voltage	± 25	V
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	A
E_{AS}	Avalanche energy, single pulsed ②	225	mJ
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	W
		$T_C = 100^\circ\text{C}$	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.65	0.78	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	45	54	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	80	--	--	V
IDSS	Zero Gate Voltage Drain Current	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_j=125^\circ\text{C}$)	$V_{DS}=80\text{V}, V_{GS}=0\text{V}$	--	--	100	μA
IGSS	Gate-Body Leakage Current	$V_{GS}=\pm 25\text{V}, V_{DS}=0\text{V}$	--	--	± 100	nA
VGS(th)	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	2.4	3.0	3.6	V
RDS(on)	Drain-Source On-State Resistance ④	$V_{GS}=10\text{V}, I_D=80\text{A}$	--	2.4	3	$\text{m}\Omega$
		$T_j=100^\circ\text{C}$	--	3	--	$\text{m}\Omega$

Dynamic Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (unless otherwise stated)

Ciss	Input Capacitance	$V_{DS}=30\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	3670	4895	6510	pF
Coss	Output Capacitance		1810	2415	3210	pF
Crss	Reverse Transfer Capacitance		25	35	60	pF
Rg	Gate Resistance	f=1MHz	0.5	0.9	5	Ω
Qg	Total Gate Charge	$V_{DS}=40\text{V}, I_D=80\text{A}, V_{GS}=10\text{V}$	--	86	114	nC
Qgs	Gate-Source Charge		--	23	31	nC
Qgd	Gate-Drain Charge		--	27	41	nC

Switching Characteristics

Td(on)	Turn-on Delay Time	$V_{DD}=40\text{V}, I_D=80\text{A}, R_G=3\Omega, V_{GS}=10\text{V}$	--	17	--	ns
Tr	Turn-on Rise Time		--	90	--	ns
Td(off)	Turn-Off Delay Time		--	45	--	ns
Tf	Turn-Off Fall Time		--	63	--	ns

Source- Drain Diode Characteristics@ $T_j= 25^\circ\text{C}$ (unless otherwise stated)

VSD	Forward on voltage	$I_{SD}=40\text{A}, V_{GS}=0\text{V}$	--	0.8	1.2	V
Trr	Reverse Recovery Time	$T_j=25^\circ\text{C}, I_{sd}=80\text{A}, V_{GS}=0\text{V}$	--	50	100	ns
		$dI/dt=100\text{A}/\mu\text{s}$	--	41	82	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax} , starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 30\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{GJA} and the maximum allowed junction temperature of 150°C .

④ Pulse width $\leq 380\mu\text{s}$; duty cycles $\leq 2\%$.

Typical Characteristics

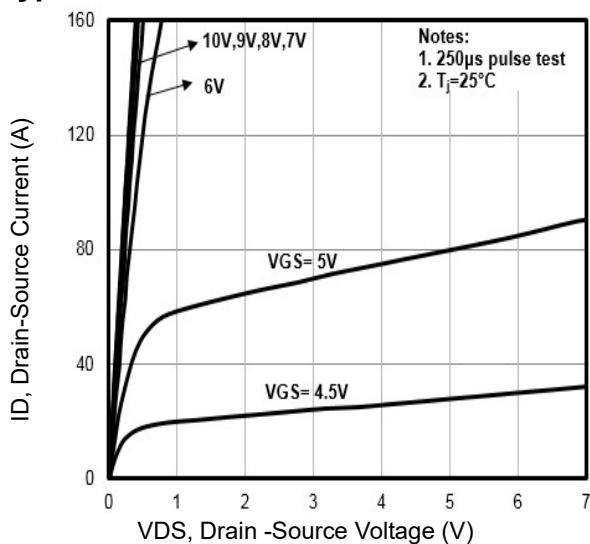


Fig1. Typical Output Characteristics

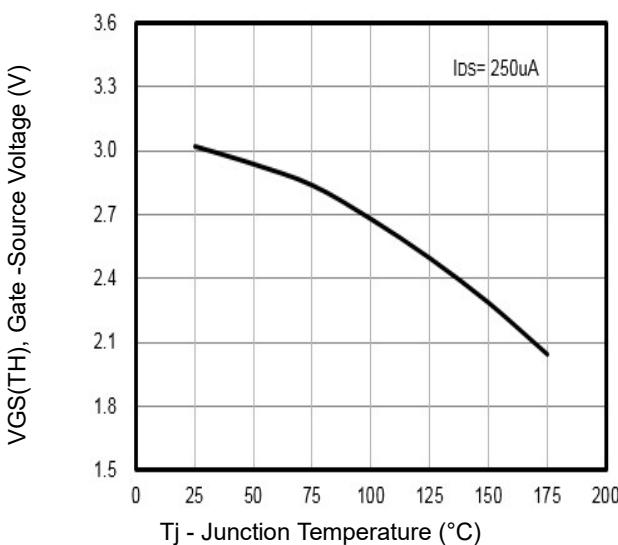


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs. T_j

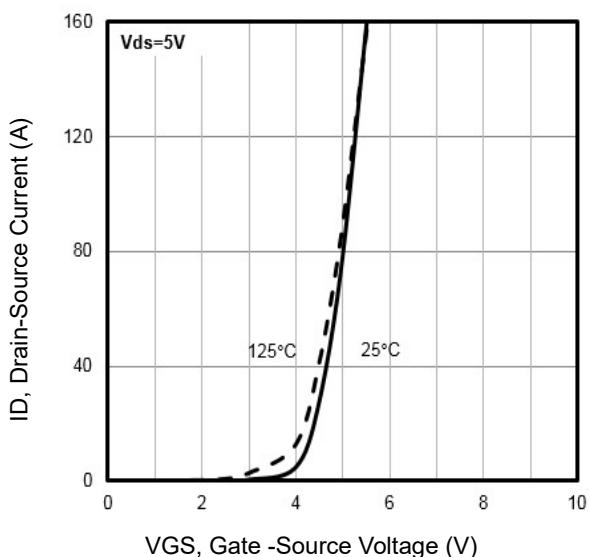


Fig3. Typical Transfer Characteristics

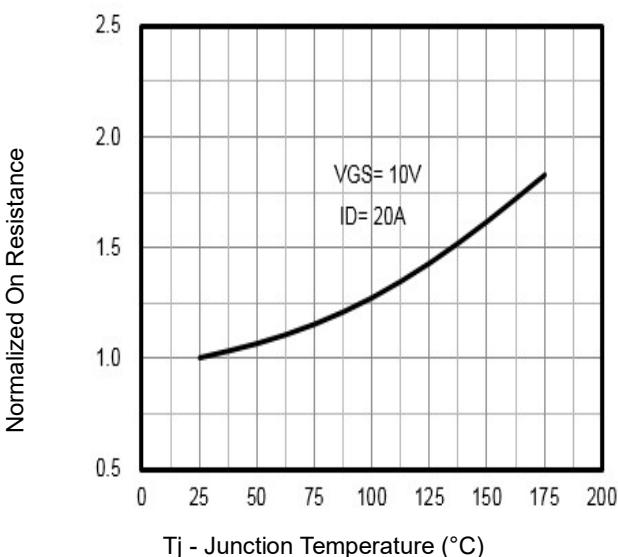


Fig4. Normalized On-Resistance Vs. T_j

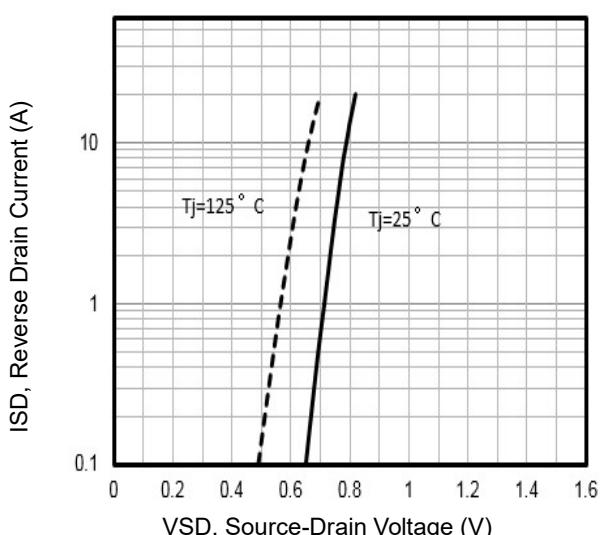


Fig5. Typical Source-Drain Diode Forward Voltage

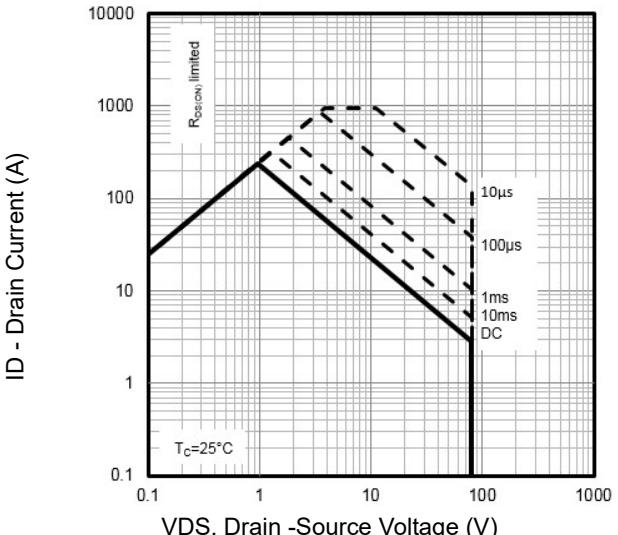


Fig6. Maximum Safe Operating Area

Typical Characteristics

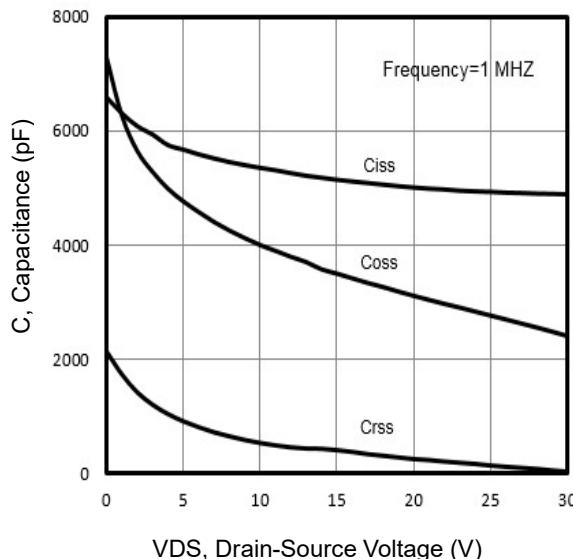


Fig7. Typical Capacitance Vs. Drain-Source Voltage

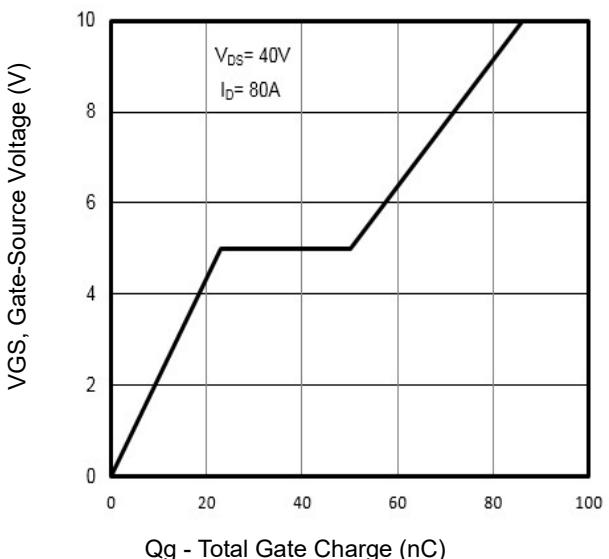


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

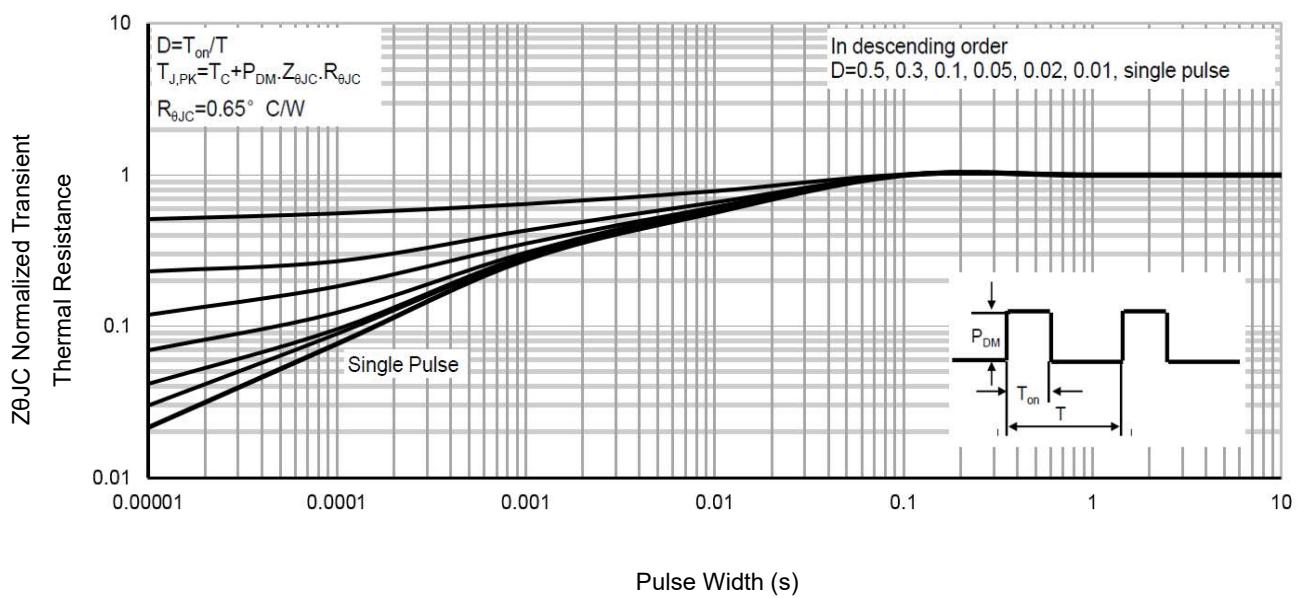


Fig9. Normalized Maximum Transient Thermal Impedance

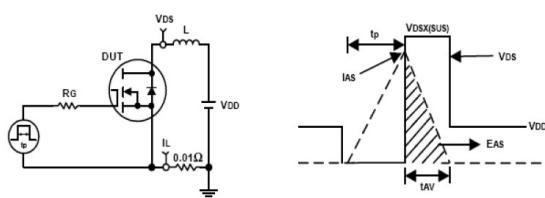


Fig10. Unclamped Inductive Test Circuit and waveforms

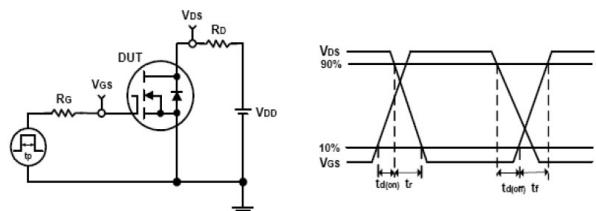
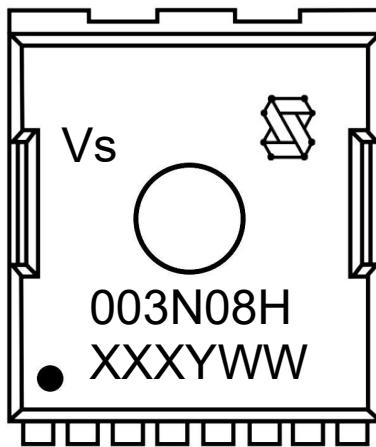


Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line: Vergiga Code (Vs) , Vergiga Logo

2nd line: Part Number (003N08H)

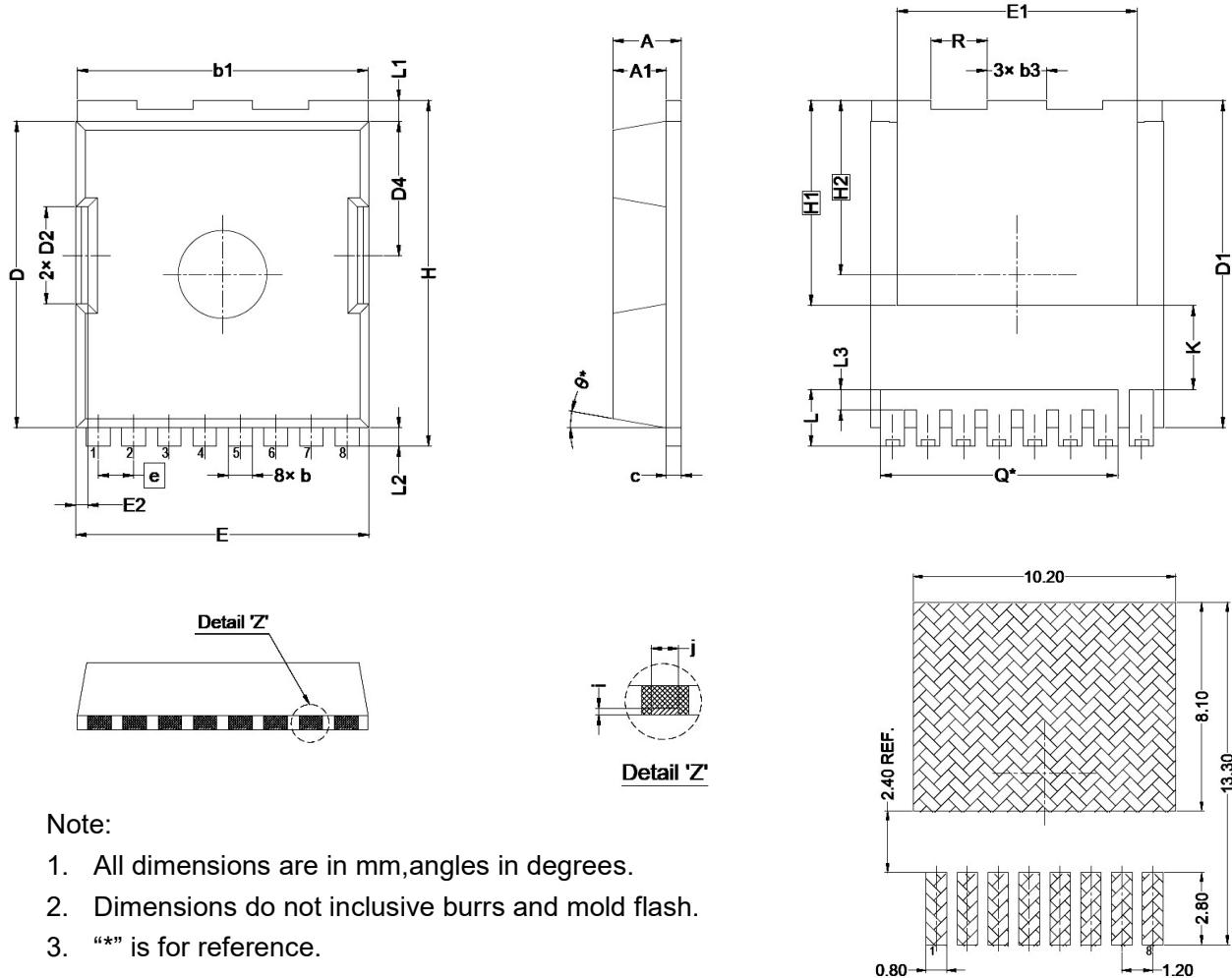
3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code , refer to table below

WW: Week Code (01 to 53)

Code	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T
Year	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030

TOLL Package Outline Data

Note:

1. All dimensions are in mm, angles in degrees.
2. Dimensions do not include burrs and mold flash.
3. “**” is for reference.

Symbol	DIMENSIONS (unit : mm)			Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max		Min	Typ	Max
A	2.20	2.30	2.40	H	11.58	11.68	11.78
A1	1.70	1.80	1.90	H1	6.95 BSC		
b	0.70	0.80	0.90	H2	5.89 BSC		
b1	9.70	9.80	9.90	i	0.10 REF		
b3	1.90	2.00	2.10	j	0.46 REF		
c	0.40	0.50	0.60	K	2.80 REF		
D	10.28	10.38	10.48	L	1.60	1.90	2.10
D1	10.98	11.08	11.18	L1	0.60	0.70	0.80
D2	3.20	3.30	3.40	L2	0.50	0.60	0.70
D4	4.45	4.55	4.65	L3	0.60	0.70	0.80
E	9.80	9.90	10.00	N	8		
E1	8.00	8.10	8.20	Q	8.00 REF		
E2	0.30	0.40	0.50	R	1.80	1.90	2.00
e	1.20 BSC			θ	10° REF		

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