

## 100V N+P-Channel Enhancement Mode MOSFET

### Description

The AP15G10GD uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

### General Features

$V_{DS} = 100V$   $I_D = 17.8A$

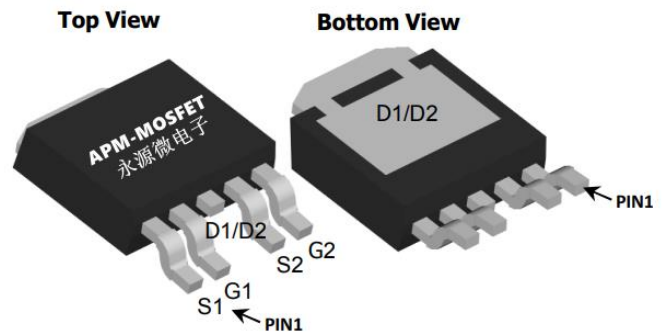
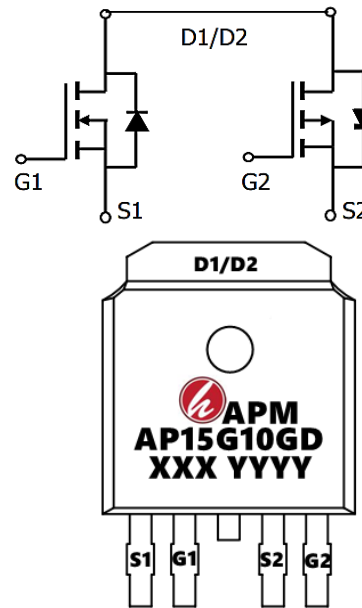
$R_{DS(ON)} < 120m\Omega$  @  $V_{GS}=10V$  (Type: 85m $\Omega$ )

$V_{DS} = -100V$   $I_D = -12.8A$

$R_{DS(ON)} < 290m\Omega$  @  $V_{GS}=-10V$  (Type: 235m $\Omega$ )

### Application

BLDC



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP15G10GD	TO-252-4L	AP15G10GD XXX YYYY	2500

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
$V_{DS}$	Drain-Source Voltage	100	-100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	17.8	12.8	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.9	-7.5	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	52.5	-38.4	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	28	18	mJ
$I_{AS}$	Avalanche Current	7	6	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	23	21.3	W
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	62.5		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	5.4		$^\circ C/W$

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### N-Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250μA	100	113	-	V
IDSS	Zero Gate Voltage Drain Current	VDS=100V, VGS=0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	VDS=0V, VGS=±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA	1.2	2.0	2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	VGS=10V, ID=5A	-	85	120	mΩ
		VGS=4.5V, ID=3A	-	95	150	mΩ
g fs	Forward Transconductance	V DS =5V , I D =5A		14		S
RG	Gate Resistance	VDS = 0V, VGS =0V,f =1MHz		3		Ω
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1.0MHz	-	1100	-	pF
Coss	Output Capacitance		-	55	-	pF
Crss	Reverse Transfer Capacitance		-	40	-	pF
Qg	Total Gate Charge	VDS=50V, ID=5A, VGS=10V	-	11.9	-	nC
Qgs	Gate-Source Charge		-	2.8	-	nC
Qgd	Gate-Drain("Miller") Charge		-	1.7	-	nC
td(on)	Turn-on Delay Time	VDS=30V, ID=5A, RG=1.8Ω, VGS=10V	-	3.8	-	ns
tr	Turn-on Rise Time		-	25.8	-	ns
td(off)	Turn-off Delay Time		-	16	-	ns
tf	Turn-off Fall Time		-	8.8	-	ns
IS	Continuous Source Current1,5	VG=VD=0V , Force Current	-	-	14.6	A
ISM	Pulsed Source Current2,5		-	-	25	A
VSD	Diode Forward Voltage2	VGS=0V, IS=10A	-	-	1.2	V

#### Note :

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.

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### P-Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

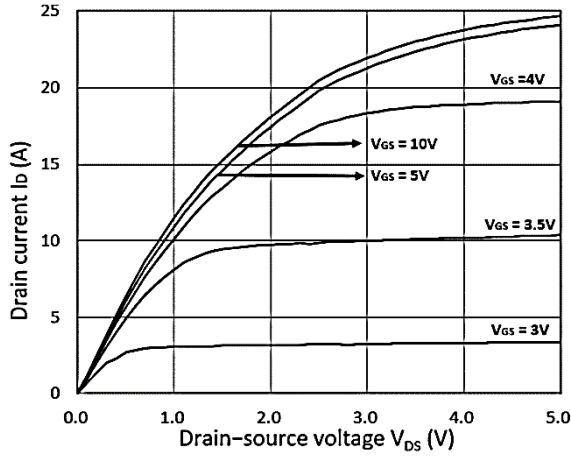
Symbol	Parameter	Test Condition	Min.	Typ	Max.	Units
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-100	117	-	V
IDSS	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -100V, V <sub>GS</sub> = 0V	-	-	1	μA
IGSS	Gate to Body Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-1.2	-1.85	-2.5	V
RDS(on)	Static Drain-Source On-Resistance <sup>note1</sup>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -5A	-	250	300	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3A	-	260	340	
Ciss	Input Capacitance	V <sub>DS</sub> = -50V, V <sub>GS</sub> = 0V, f = 1.0MHz	-	760	-	pF
Coss	Output Capacitance		-	25	-	pF
Crss	Reverse Transfer Capacitance		-	12	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> = -50V, I <sub>D</sub> = -5A, V <sub>GS</sub> = -10V	-	11.5	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.3	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	2.9	-	nC
td(on)	Turn-On Delay Time	V <sub>DS</sub> = -50V, I <sub>D</sub> = -5A R <sub>G</sub> =4.5Ω, R <sub>L</sub> =25Ω V <sub>GEN</sub> = -10 V	-	12	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	5	-	ns
td(off)	Turn-Off Delay Time		-	35	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	20	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-12.8	A
VSD	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1A	-	-	-1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>sd</sub> = -3A, di/dt =100A/μs	-	25	-	nS
Q <sub>rr</sub>	Reverse Recovery Charge		-	20	-	nC

**Note :**

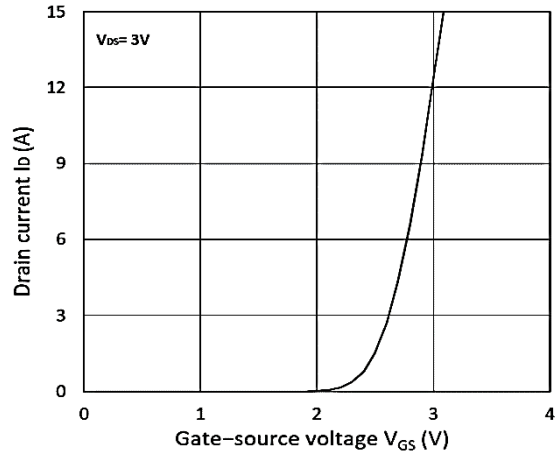
1. The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width .The EAS data shows Max. rating .
3. The power dissipation is limited by 175°C junction temperature
4. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>= -24V, V<sub>G</sub>= -10V, R<sub>G</sub>=7Ω, L=0.1mH, I<sub>AS</sub>= -29.5A
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

**100V N+P-Channel Enhancement Mode MOSFET**

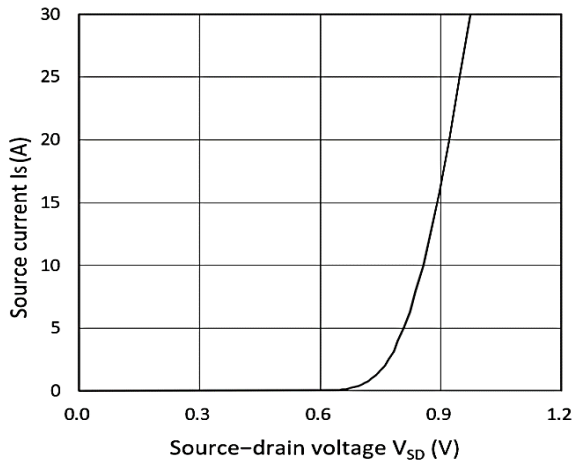
**N-Typical Characteristics**



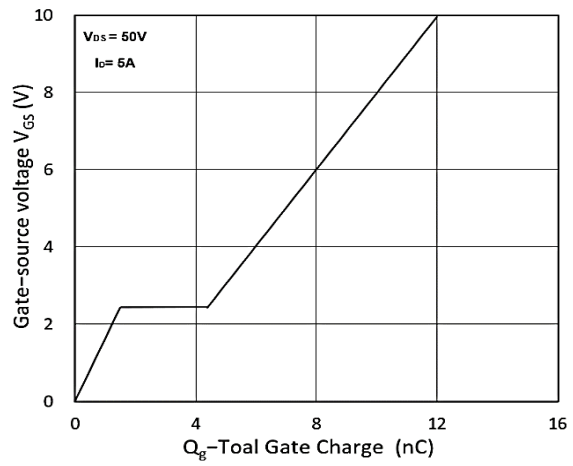
**Figure 1. Output Characteristics**



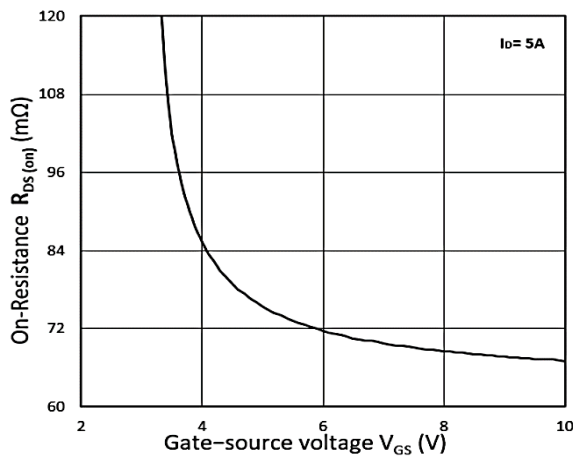
**Figure 2. Transfer Characteristics**



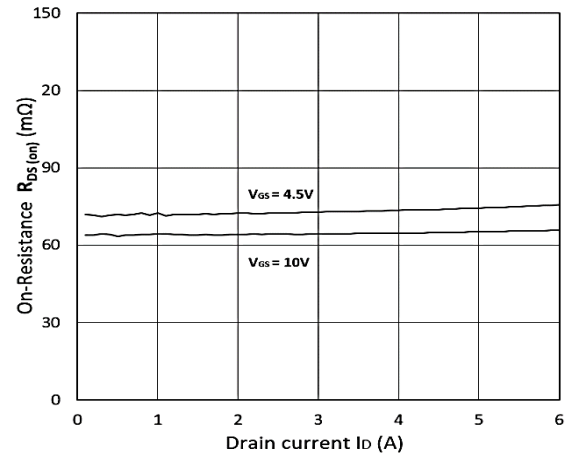
**Figure 3. Forward Characteristics of Reverse**



**Figure 4. Gate Charge Characteristics**



**Figure 5.  $R_{DS(on)}$  vs.  $V_{GS}$**



**Figure 6.  $R_{DS(on)}$  vs.  $I_D$**

## 100V N+P-Channel Enhancement Mode MOSFET

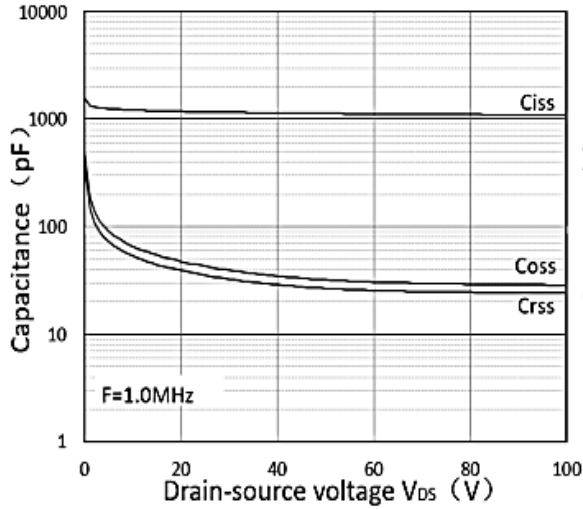


Figure 7. Capacitance Characteristics

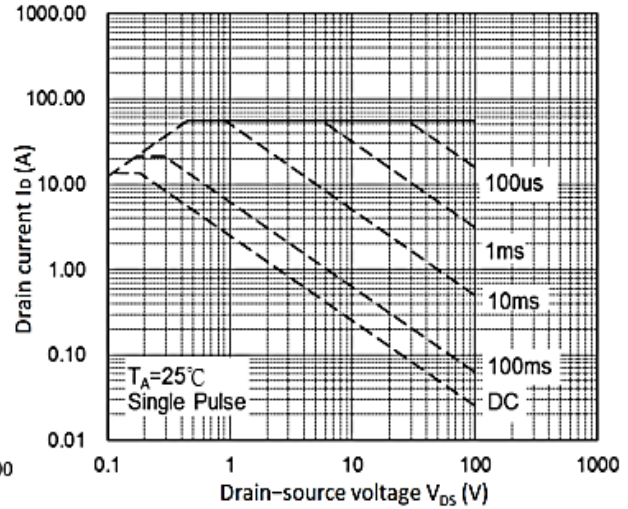


Figure 8. Safe Operating Area

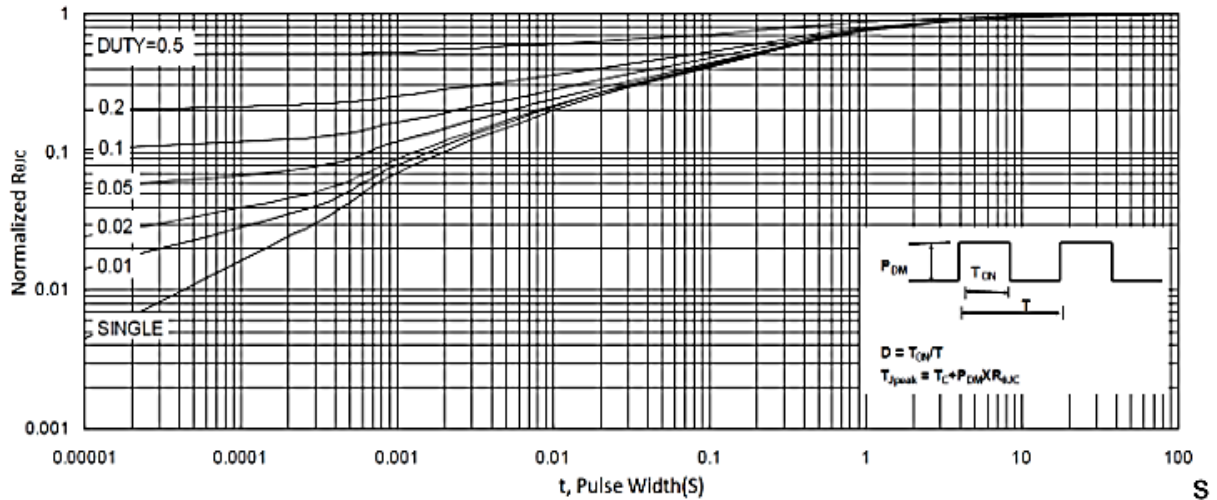


Figure 9. Normalized Maximum Transient Thermal Impedance

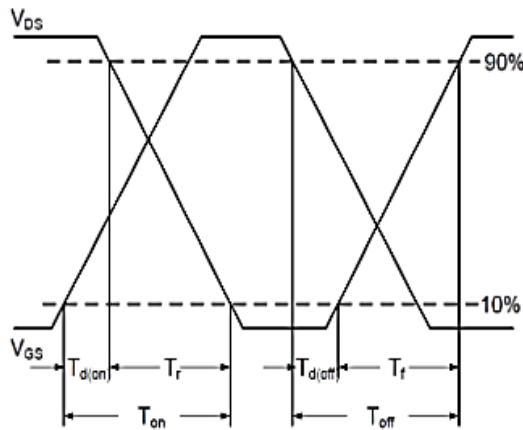


Figure 10. Switching Time Waveform

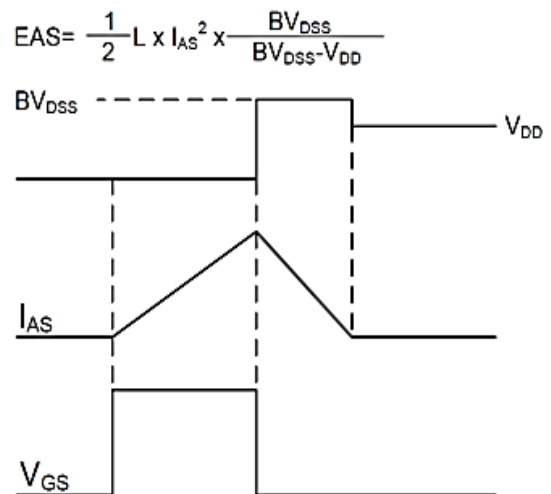


Figure 11. Unclamped Inductive Switching Waveform

## 100V N+P-Channel Enhancement Mode MOSFET

### P-Typical Characteristics

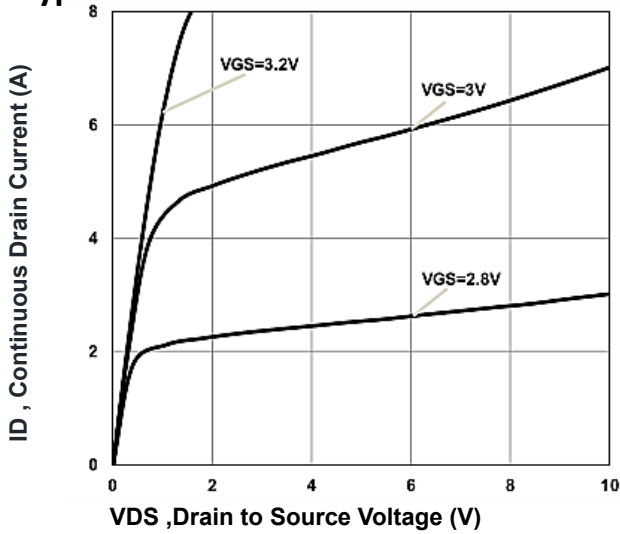


Figure 1. Typical Output Characteristics

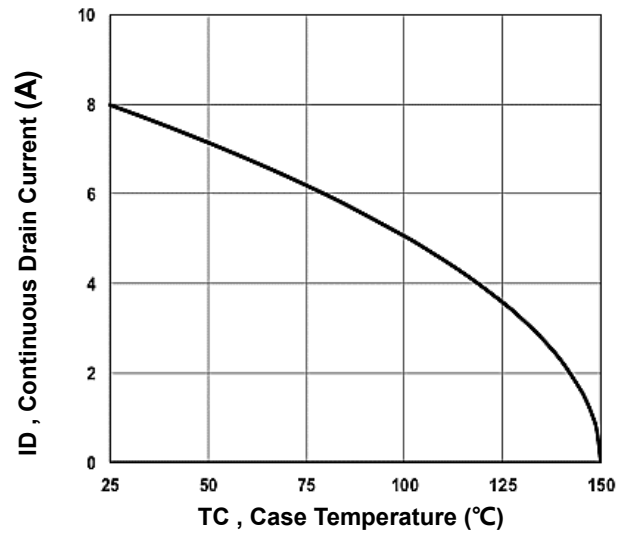


Figure 2. Continuous Drain Current vs.  $T_C$

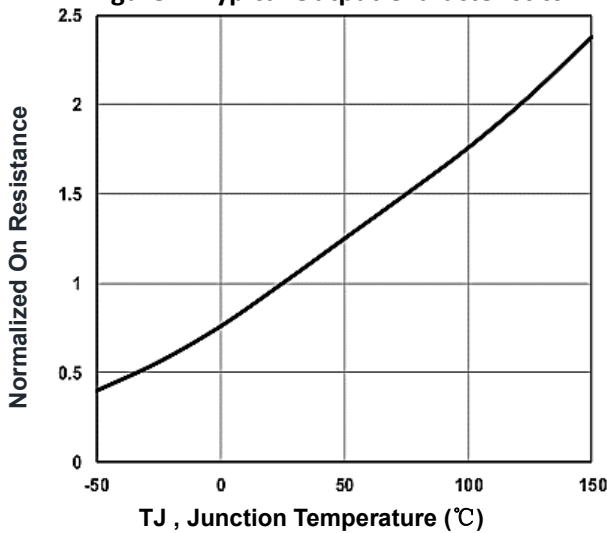


Figure 3. Normalized  $R_{DS(on)}$  vs.  $T_J$

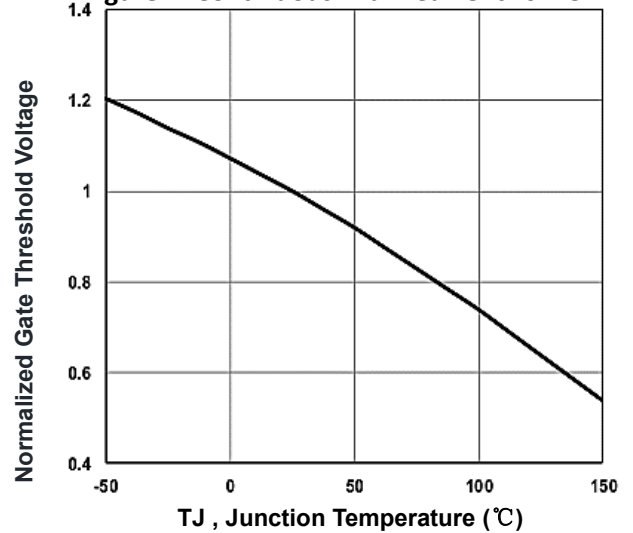


Figure 5. Normalized  $V_{th}$  vs.  $T$

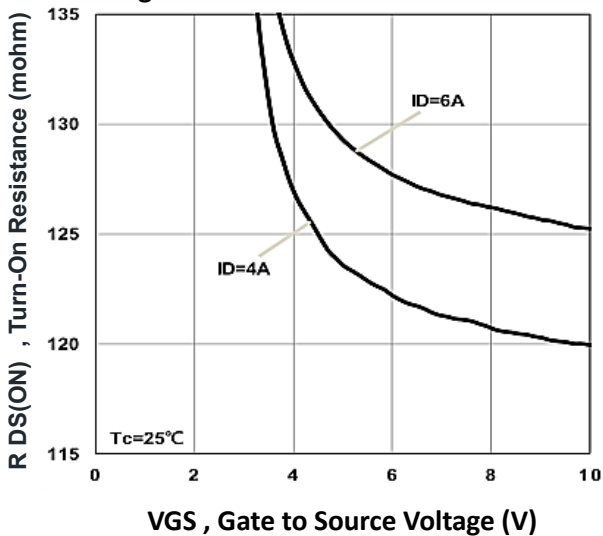


Figure 6. Turn-On Resistance vs.  $V_{GS}$

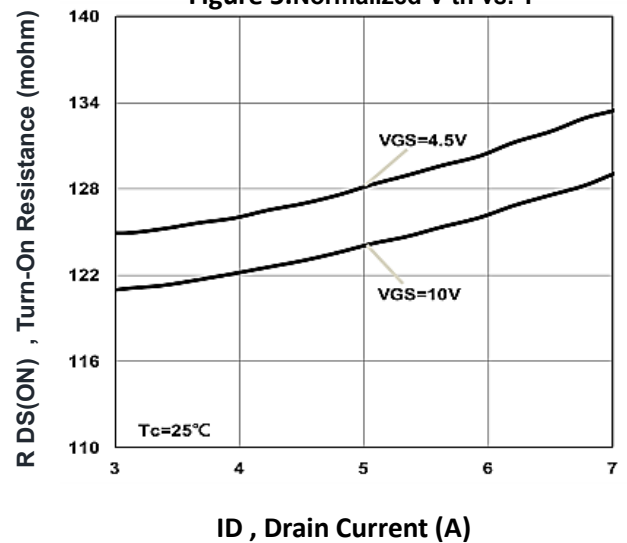
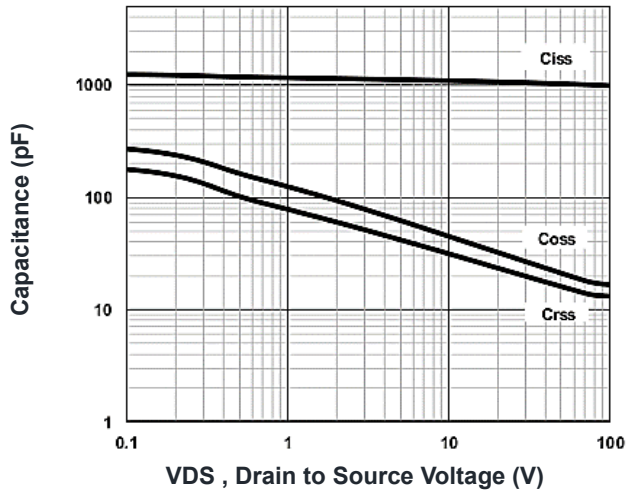
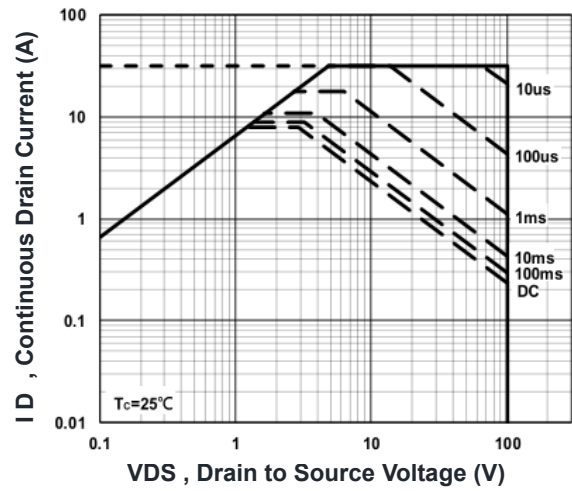


Figure 7. Turn-On Resistance vs.  $I_D$

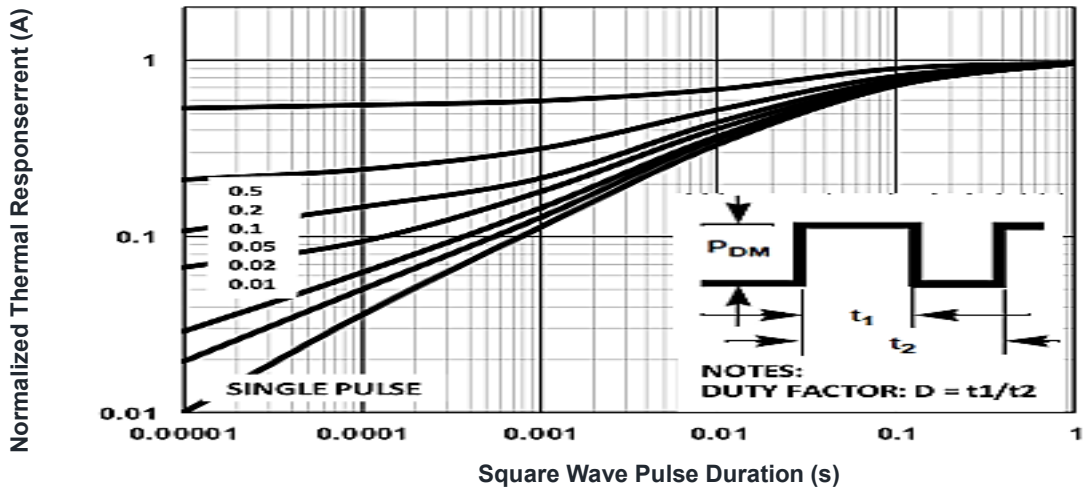
## 100V N+P-Channel Enhancement Mode MOSFET



VDS , Drain to Source Voltage (V)  
Figure 8. Capacitance Characteristics



VDS , Drain to Source Voltage (V)  
Figure 9. Maximum Safe Operation Area



Square Wave Pulse Duration (s)  
Figure 10. Normalized Transient Impedance

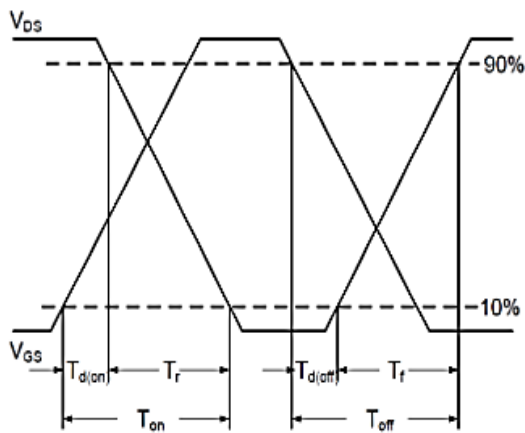


Figure 10. Switching Time Waveform

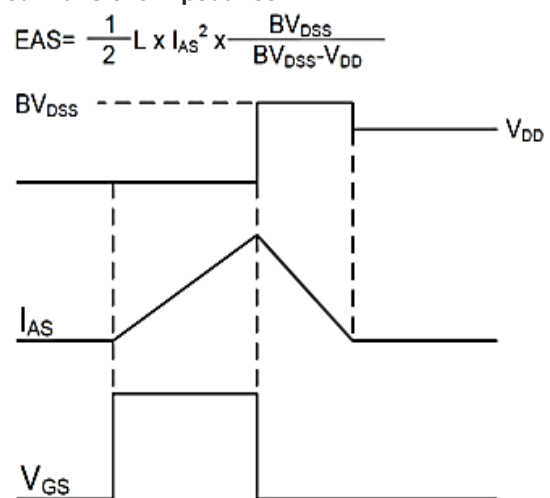
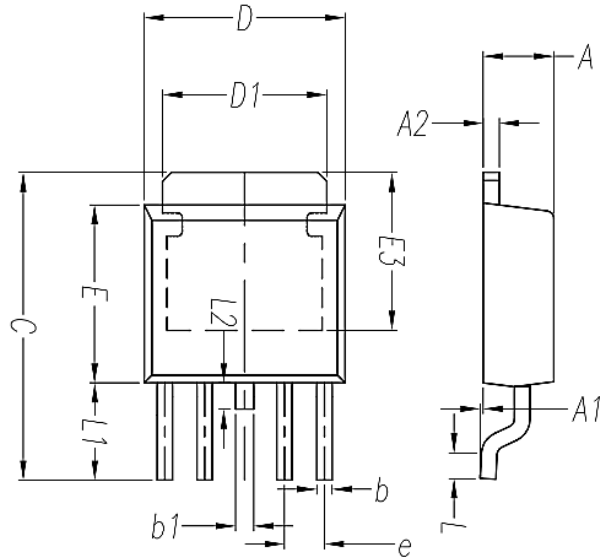


Figure 11. Unclamped Inductive Switching Waveform



### Package Mechanical Data-TO-252-4L-Duble-DX



Symbol	Common		
	mm		
	Mim	Nom	Max
D	6.30	6.55	6.80
D1	4.80	5.35	5.90
C	9.70	10.00	10.30
E	5.90	6.10	6.30
E3	4.50	5.15	5.80
L	0.90	1.35	1.80
L1	2.60	2.85	3.05
L2	0.50	0.85	1.20
b	0.30	0.50	0.70
b1	0.40	0.60	0.80
A	2.10	2.30	2.50
A2	0.40	0.53	0.65
A1	0.00	0.10	0.20
e	1.17	1.27	1.37



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Edition	Date	Change
Rve1.0	2022/3/10	Initial release

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