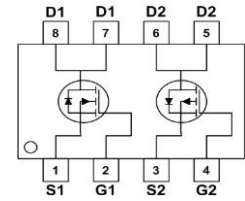


## 60V N+P-Channel Enhancement Mode MOSFET

### Description

The AP5G06S uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



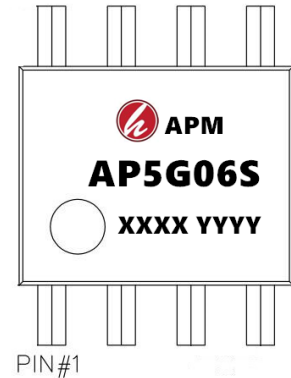
### General Features

$V_{DS} = 60V$   $I_D = 4.8 A$

$R_{DS(ON)} < 32m\Omega$  @  $V_{GS}=10V$

$V_{DS} = -60V$   $I_D = -3.7 A$

$R_{DS(ON)} < 70m\Omega$  @  $V_{GS}=10V$



### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP5G06S	SOP-8	AP5G06S XXXX YYYY	2500

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
$V_{DS}$	Drain-Source Voltage	60	-60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.8	-3.7	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	3.8	-3	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	9.6	-7.5	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	25.5	35.3	mJ
$I_{AS}$	Avalanche Current	22.6	-26.6	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation <sup>4</sup>	1.5	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	85	$^\circ\text{C/W}$

## 60V N+P-Channel Enhancement Mode MOSFET

R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	---	36	°C/W
------------------	---	-----	----	------

### Absolute Maximum Ratings (T<sub>c</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.063	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =4A	---	---	32	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =2A	---	---	38	
V <sub>GS(th)</sub>	Gate Threshold Voltage		1.2	---	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	---	-5.24	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =48V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =4A	---	21	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	3.2	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)		---	12.6	---	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =48V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =4A	---	3.2	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	6.3	---	
T <sub>d(on)</sub>	Turn-On Delay Time		---	8	---	ns
T <sub>r</sub>	Rise Time	V <sub>DD</sub> =30V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =4A	---	14.2	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	24.4	---	
T <sub>f</sub>	Fall Time		---	4.6	---	
C <sub>iss</sub>	Input Capacitance		---	1378	---	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	86	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	64	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>		---	---	4.8	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	9.6	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

#### Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=-25V,V<sub>GS</sub>=-10V,L=0.1mH,I<sub>AS</sub>=-26.6A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation

## 60V N+P-Channel Enhancement Mode MOSFET

### Absolute Maximum Ratings ( $T_c=25^\circ\text{C}$ unless otherwise noted)

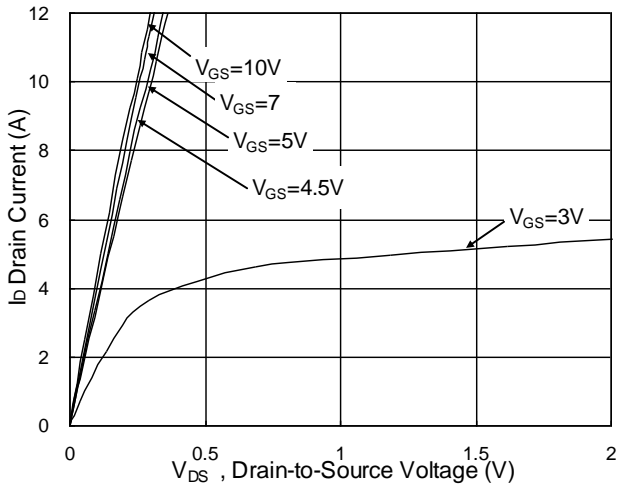
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.03	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-3A$	---	---	70	m $\Omega$
		$V_{GS}=-4.5V, I_D=-2A$	---	---	105	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	---	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.56	---	mV/ $^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu\text{A}$
		$V_{DS}=-48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-3A$	---	15	---	S
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	13.5	---	$\Omega$
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-48V, V_{GS}=-4.5V, I_D=-3A$	---	9.86	---	nC
$Q_{gs}$	Gate-Source Charge		---	3.1	---	
$Q_{gd}$	Gate-Drain Charge		---	2.95	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_g=3.3, I_D=-1A$	---	28.8	---	ns
$T_r$	Rise Time		---	19.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	60.8	---	
$T_f$	Fall Time		---	7.2	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	1447	---	pF
$C_{oss}$	Output Capacitance		---	97.3	---	
$C_{riss}$	Reverse Transfer Capacitance		---	70	---	
$I_s$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	-3.7	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	-7.5	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_s=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

Note :

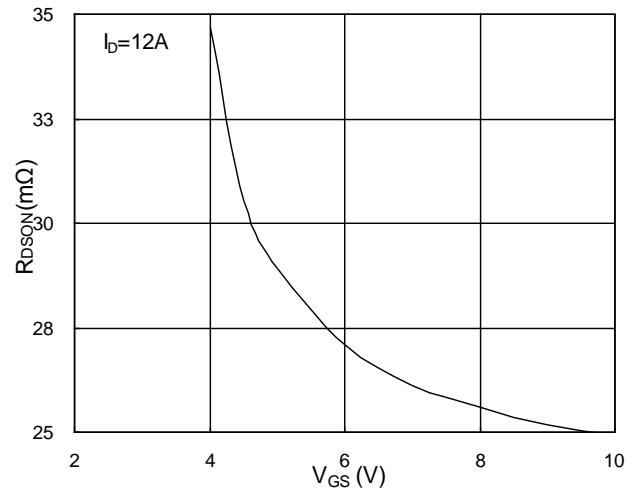
- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=22.6A$
- 4.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation

**60V N+P-Channel Enhancement Mode MOSFET**

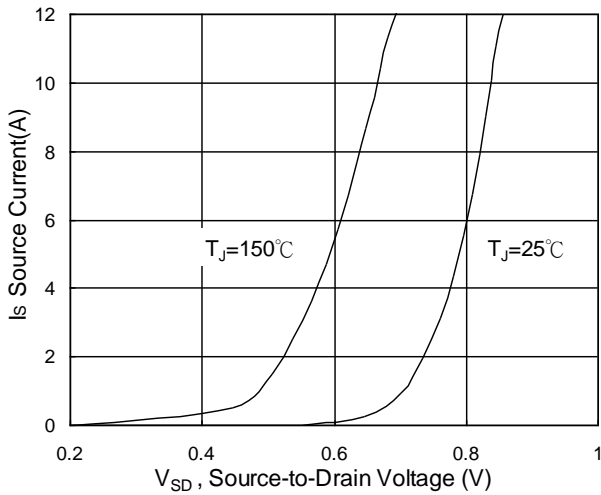
**N-Channel Typical Characteristics**



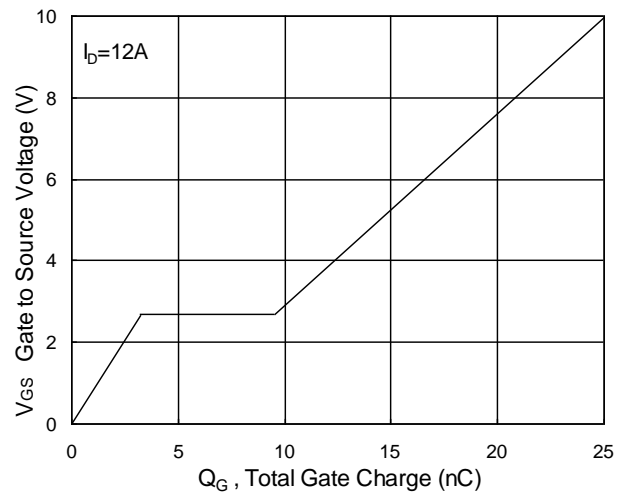
**Fig.1 Typical Output Characteristics**



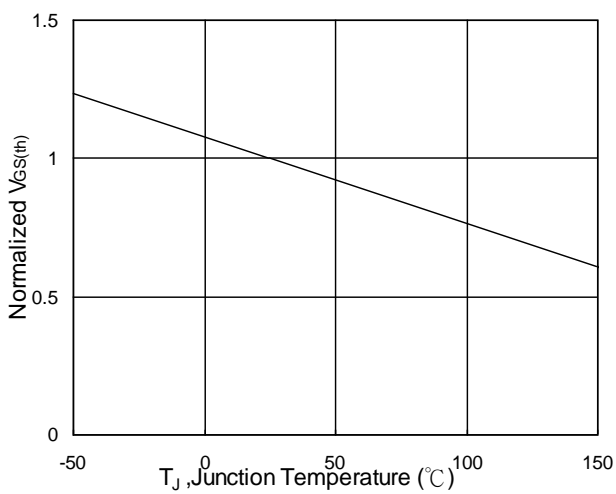
**Fig.2 On-Resistance v.s Gate-Source**



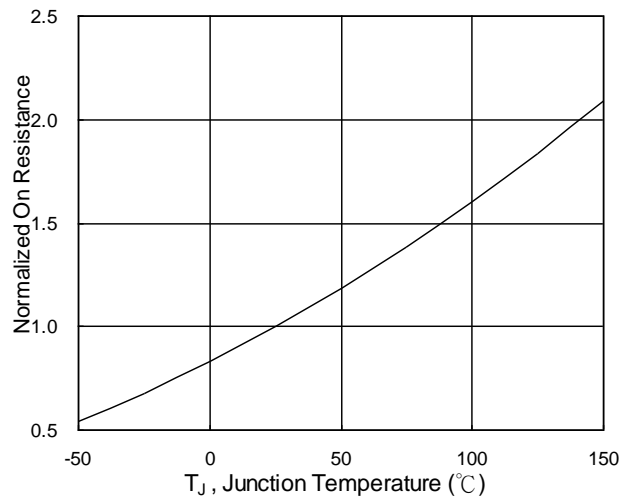
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

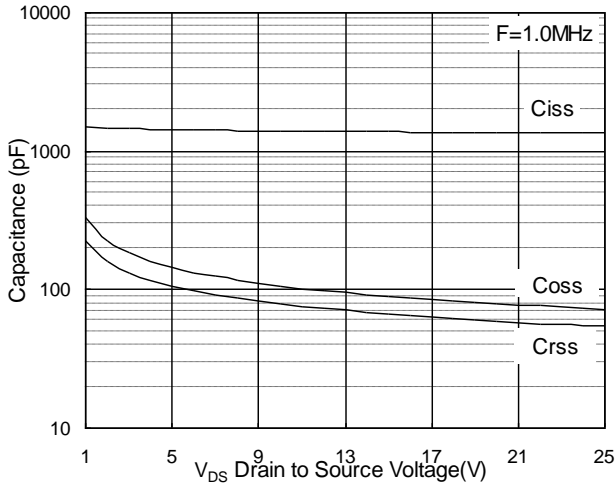


**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**

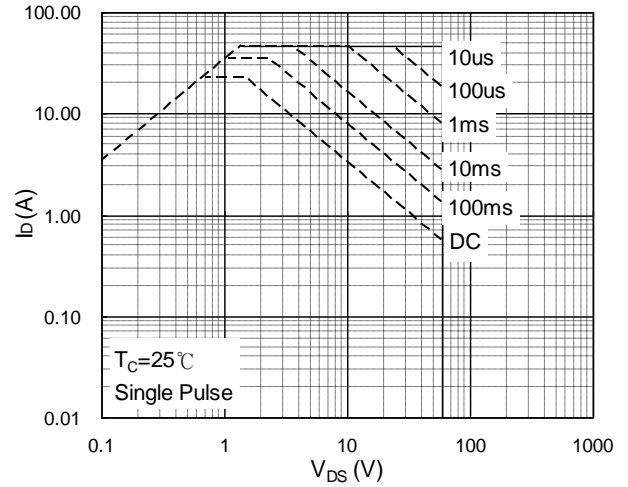


**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**

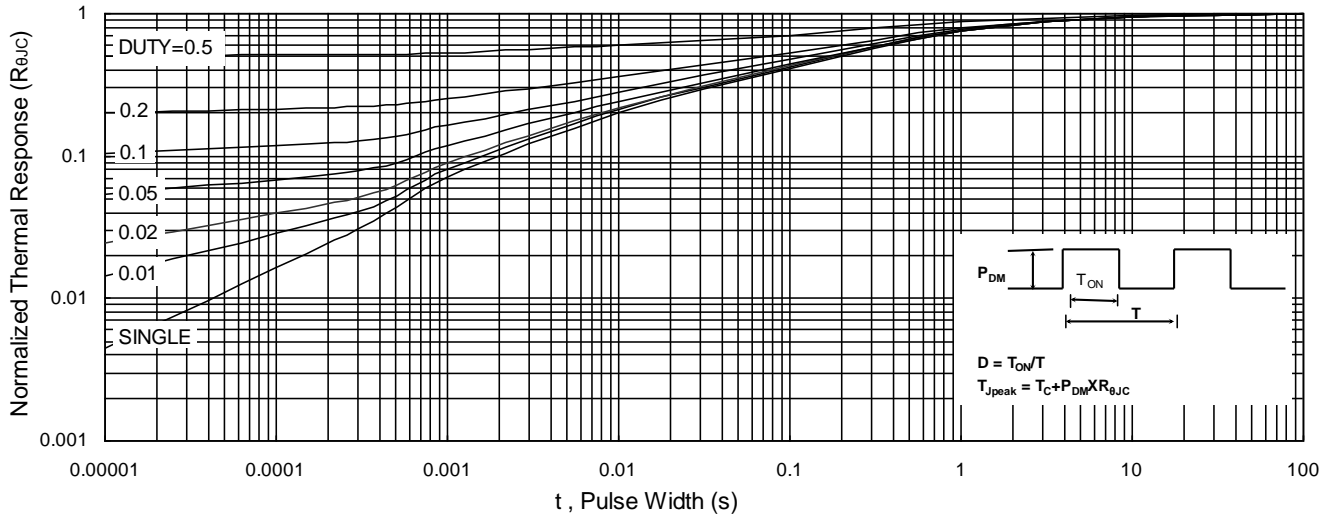
**60V N+P-Channel Enhancement Mode MOSFET**



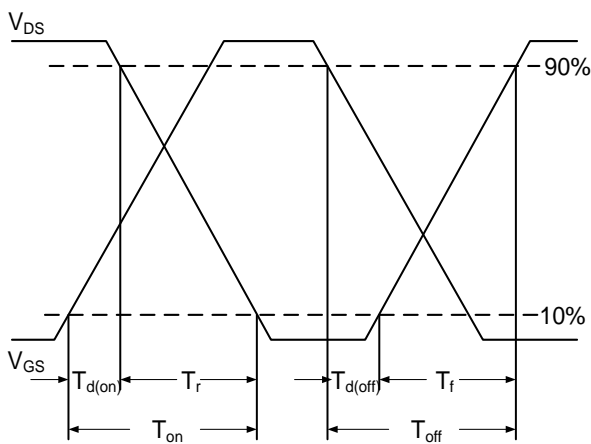
**Fig.7 Capacitance**



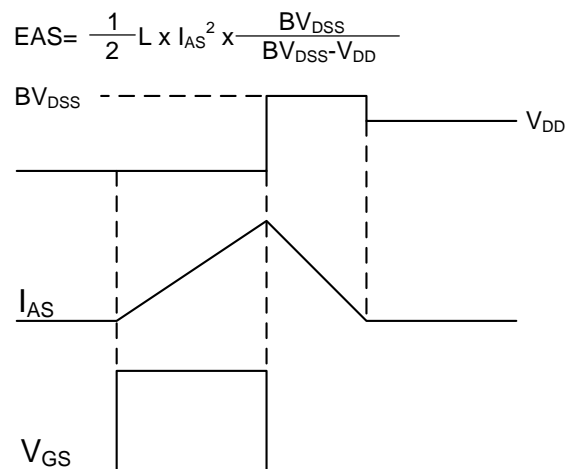
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



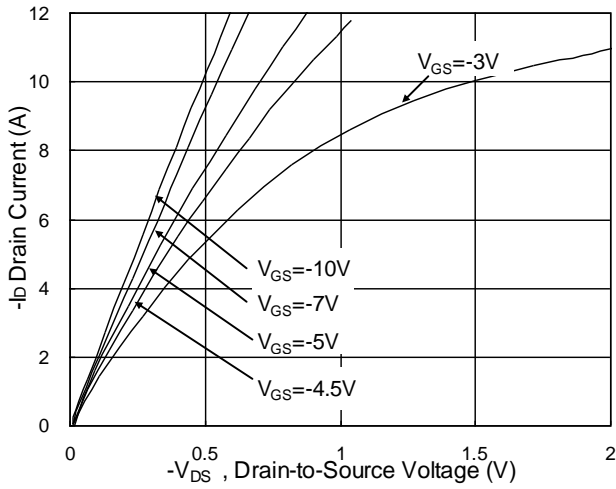
**Fig.10 Switching Time Waveform**



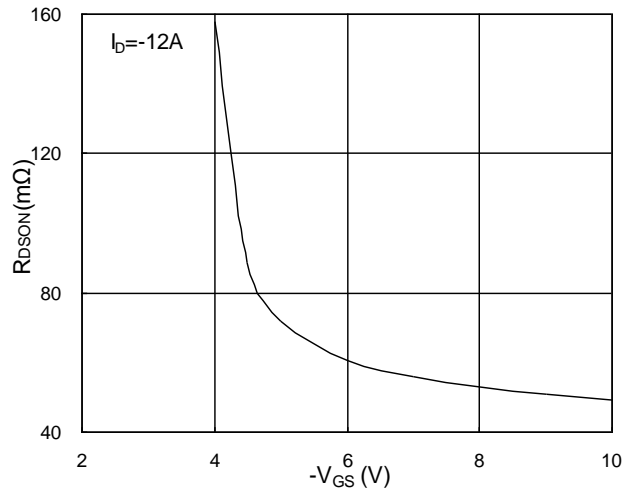
**Fig.11 Unclamped Inductive Waveform**

**60V N+P-Channel Enhancement Mode MOSFET**

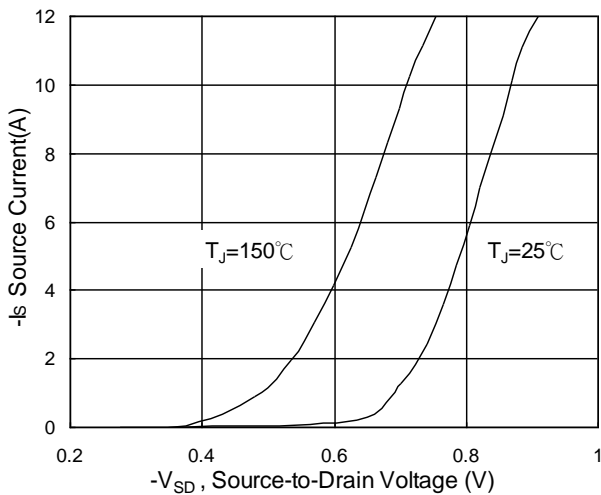
**P-Channel Typical Characteristics**



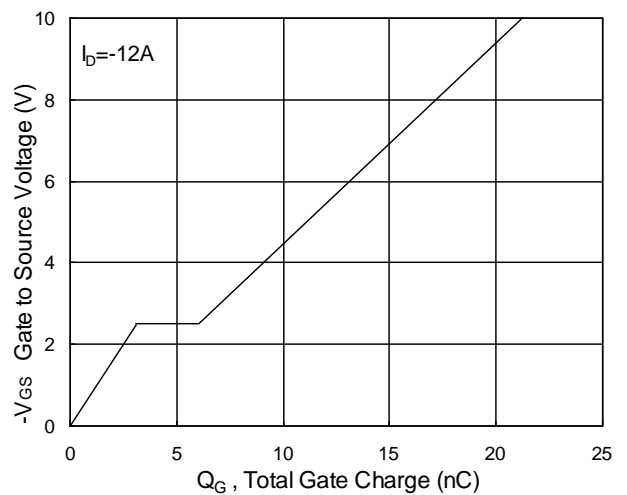
**Fig.1 Typical Output Characteristics**



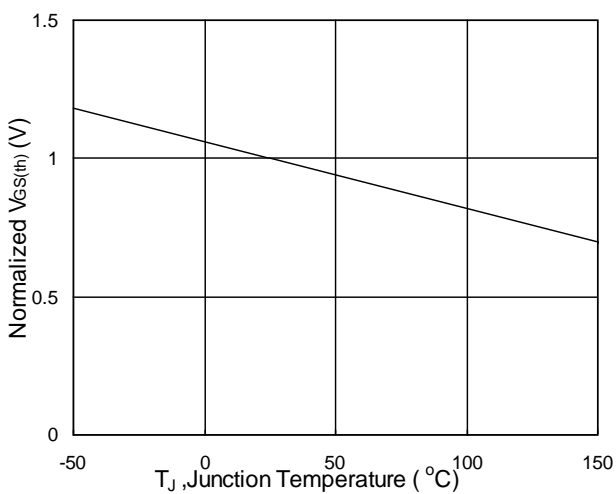
**Fig.2 On-Resistance v.s Gate-Source**



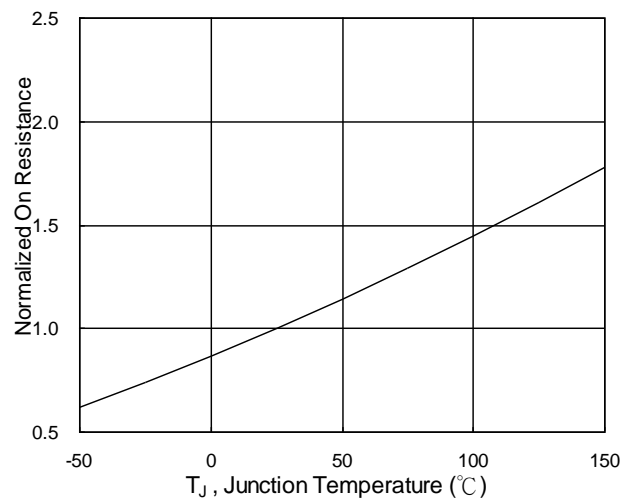
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

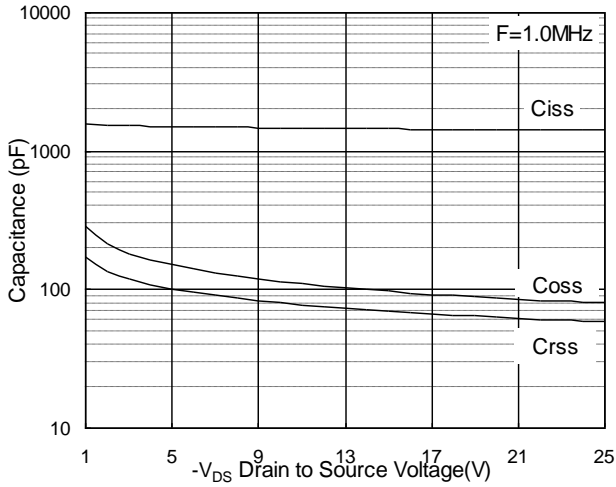


**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_j$**

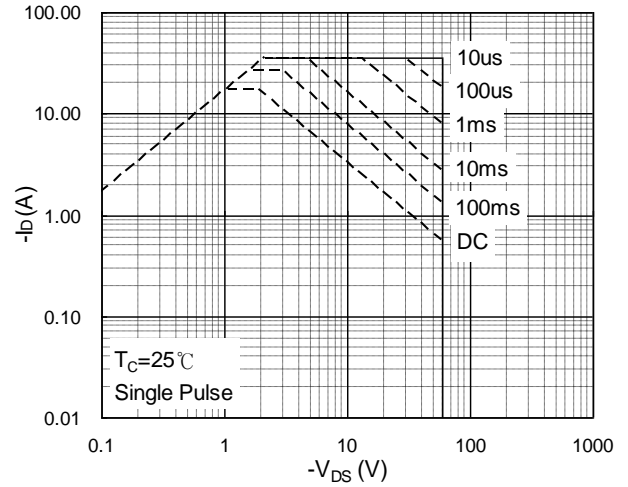


**Fig.6 Normalized  $R_{DSON}$  v.s  $T_j$**

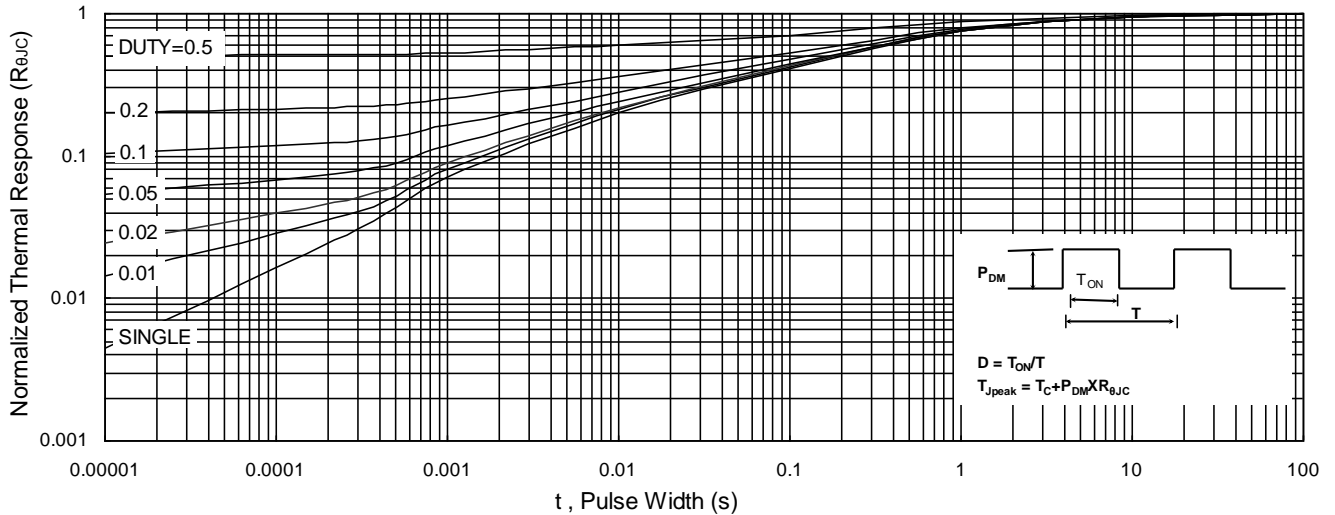
**60V N+P-Channel Enhancement Mode MOSFET**



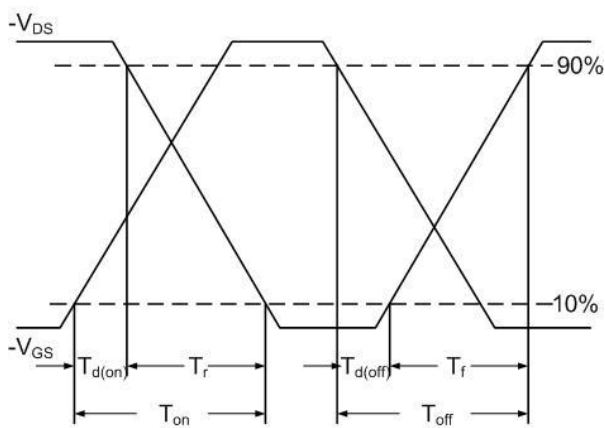
**Fig.7 Capacitance**



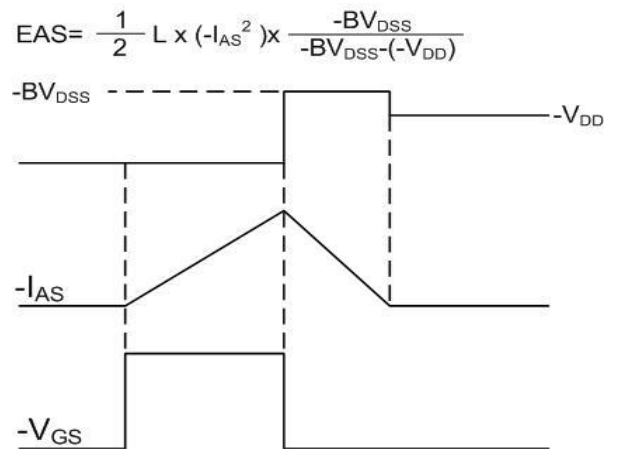
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**

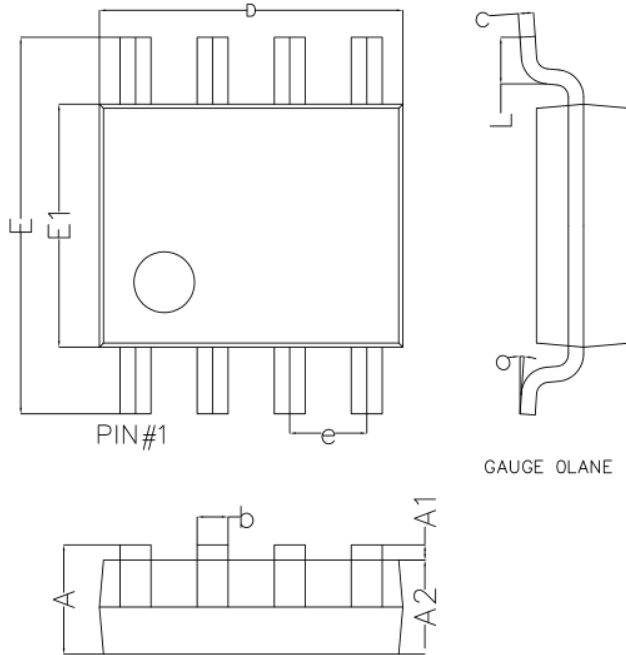


**Fig.11 Unclamped Inductive Waveform**



## 60V N+P-Channel Enhancement Mode MOSFET

SOP8 Package outline



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°



**60V N+P-Channel Enhancement Mode MOSFET****Attention**

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