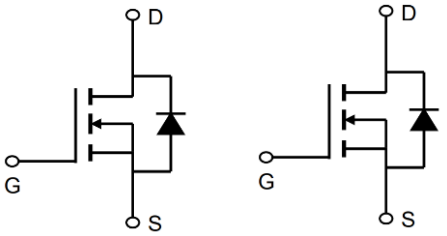
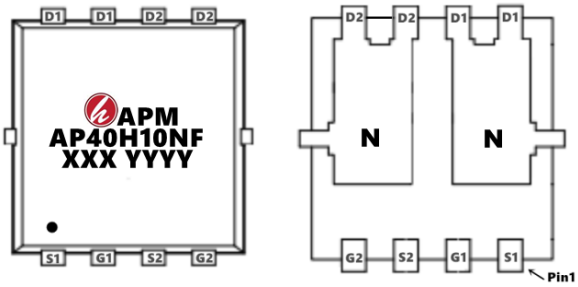
# AP40H10NF

## 100V N+N-Channel Enhancement Mode MOSFET

### Description

The AP40H10NF uses advanced **APM-SGT II** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.




### General Features

$V_{DS}$ = 100V $I_D$ =40A

$R_{DS(ON)}$ < 20mΩ @ $V_{GS}$=10V （Type：14mΩ）

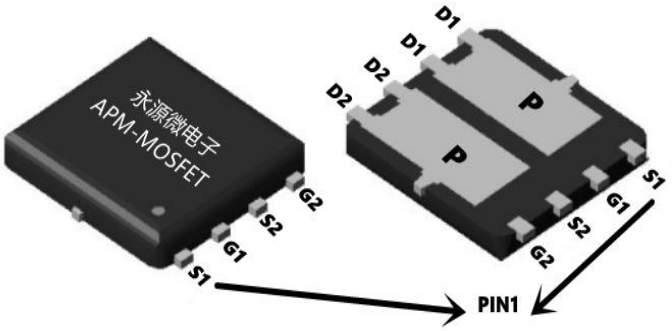
### Application

Consumer electronic power supply

Motor control

Synchronous-rectification

Isolated DC




### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| AP40H10NF | PDFN5*6-8L | AP40H10NF XXX YYYY | 5000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| VDS | Drain source voltage | 100 | V |
| VGS | Gate source voltage | ±20 | V |
| ID | Continuous drain current[1], $T_C$=25 ℃ | 40 | A |
| ID, pulse | Pulsed drain current[2], $T_C$=25 ℃ | 120 | A |
| $P_D$ | Power dissipation[3], $T_C$=25 ℃ | 71 | W |
| EAS | Single pulsed avalanche energy[5] | 57 | mJ |
| Tstg，Tj | Operation and storage temperature | -55 to 150 | ℃ |
| RθJC | Thermal resistance, junction-case | 1.76 | ℃/W |
| RθJA | Thermal resistance, junction-ambient[4] | 25 | °C/W |

## Electrical Characteristics ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| BVDSS | Drain-source breakdown voltage | $V_{GS}$=0 V, $I_D$=250 μA | 100 | 107 | | V |
| VGS(th) | Gate threshold voltage | $V_{DS}$=$V_{GS}$, $I_D$=250 μA | 1.2 | 1.5 | 2.5 | V |
| RDS(ON) | Drain-source on-state resistance | $V_{GS}$=10 V, $I_D$=10 A | | 14 | 20 | mΩ |
| RDS(ON) | Drain-source on-state resistance | $V_{GS}$=4.5 V, $I_D$=7 A | | 18 | 25 | mΩ |
| IGSS | Gate-source leakage current | $V_{GS}$=±20 V | | | ±100 | nA |
| IDSS | Drain-source leakage current | $V_{DS}$=100 V, $V_{GS}$=0 V | | | 1 | uA |
| Ciss | Input capacitance | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=100 kHz | | 1003.9 | | pF |
| Coss | Output capacitance | | | 185.4 | | pF |
| Crss | Reverse transfer capacitance | | | 9.8 | | pF |
| td(on) | Turn-on delay time | $V_{GS}$=10 V, $V_{DS}$=50 V, $R_G$=10 Ω, $I_D$=5 A | | 16.6 | | ns |
| $t_r$ | Rise time | | | 3.8 | | ns |
| td(off) | Turn-off delay time | | | 75.5 | | ns |
| $t_f$ | Fall time | | | 46 | | ns |
| $Q_g$ | Total gate charge | $I_D$=5 A, $V_{DS}$=50V, $V_{GS}$=10V | | 16.2 | | nc |
| $Q_{gs}$ | Gate-source charge | | | 2.8 | | nc |
| Qgd | Gate-drain charge | | | 4.1 | | nc |
| Vplateau | Gate plateau voltage | | | 3 | | V |
| $I_S$ | Diode forward current | VGS<Vth | | 30 | | A |
| ISP | Pulsed source current | | | 90 | | A |
| trr | Reverse recovery time | $I_S$=1A, di/dt=100 A/μs | 49 | | | ns |
| $Q_{rr}$ | Reverse recovery charge | | 61.8 | | | nc |
| Irrm | Peak reverse recovery current | | 2.4 | | | A |

**Note :**

1、Calculated continuous current based on maximum allowable junction temperature.
2、Repetitive rating; pulse width limited by max. junction temperature.
3、Pd is based on max. junction temperature, using junction-case thermal resistance.
4、The value of $R_{\Theta ja}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a$=25 °C.
5、$V_{DD}$=50 V, $R_G$=25 Ω, L=0.3 mH, starting $T_j$=25 °C.

## Typical Characteristics

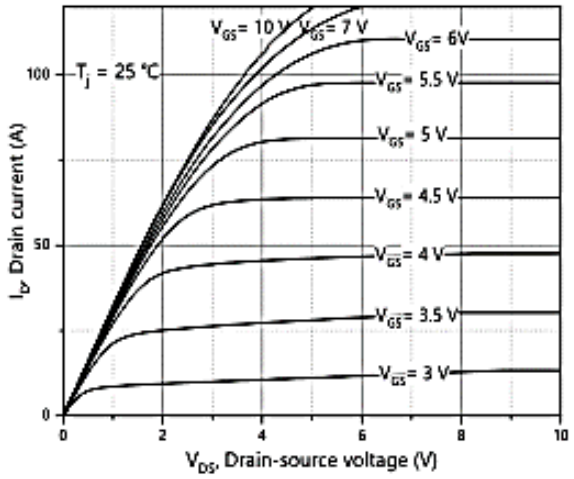



Figure 1, Typ. output characteristics

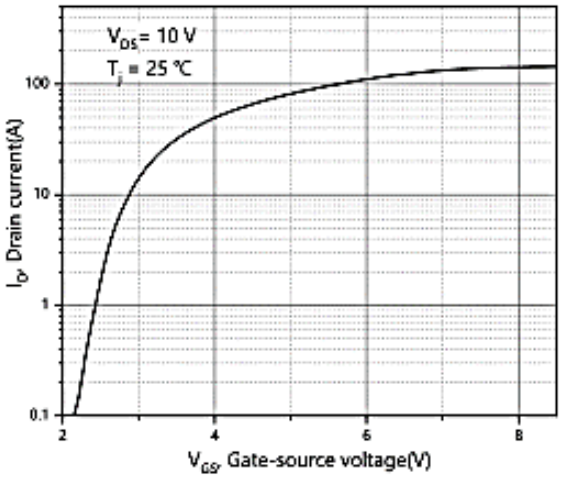



Figure 2, Typ. transfer characteristics

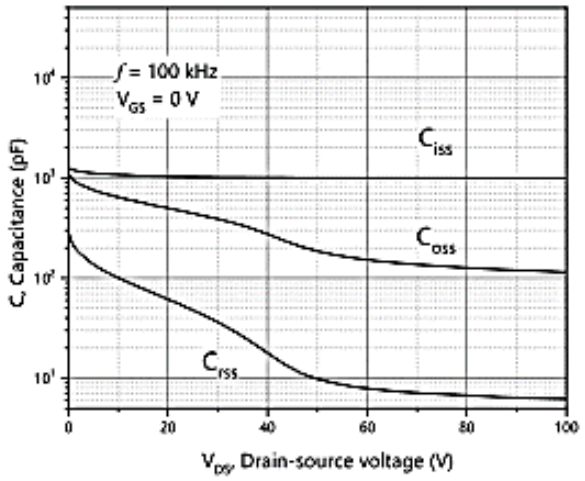



Figure 3, Typ. capacitances

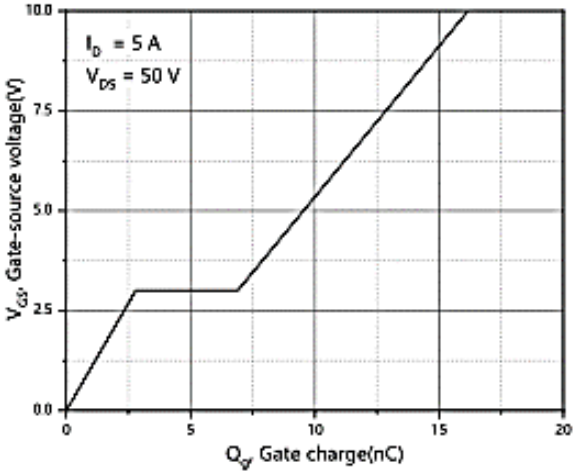



Figure 4, Typ. gate charge

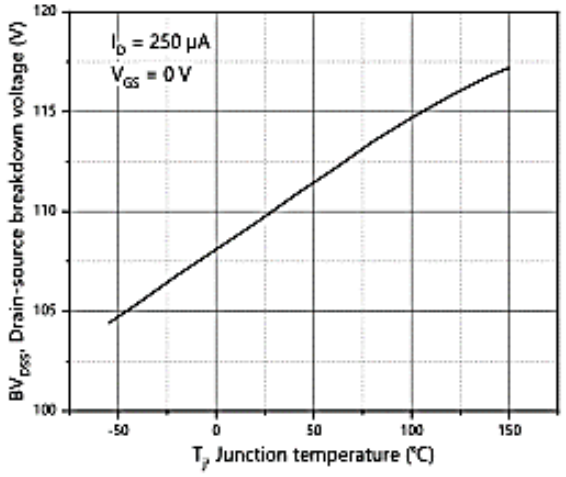



Figure 5, Drain-source breakdown voltage

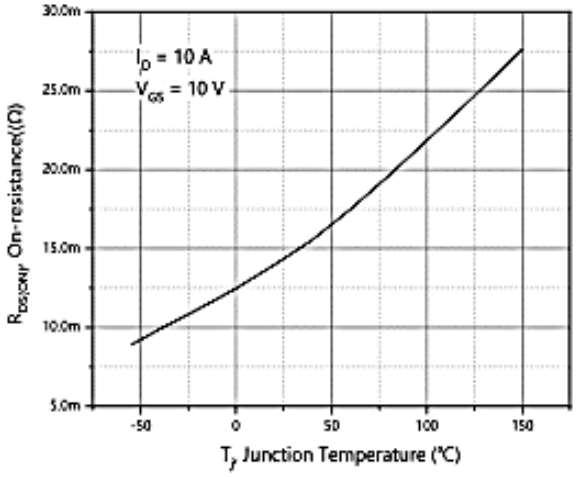



Figure 6, Drain-source on-state resistance

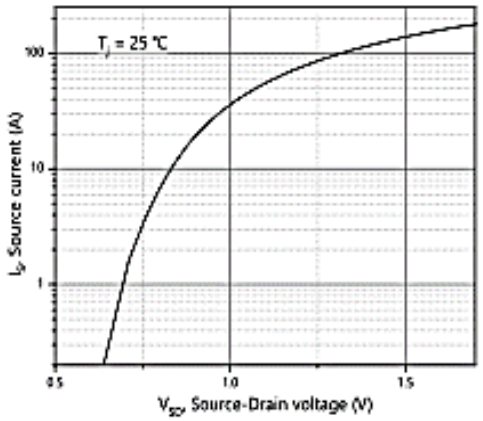



Figure 7, Forward characteristic of body diode

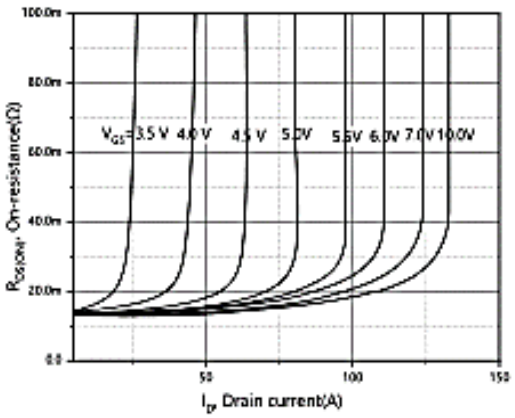



Figure 8, Drain-source on-state resistance

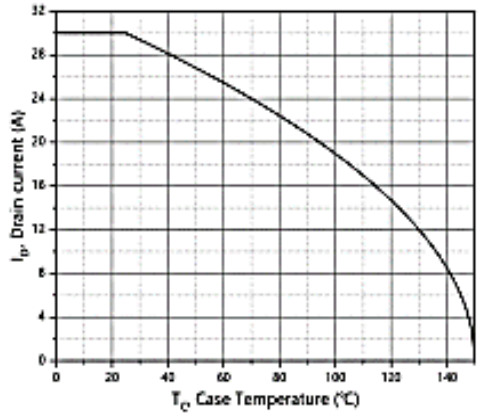



Figure 9, Drain current

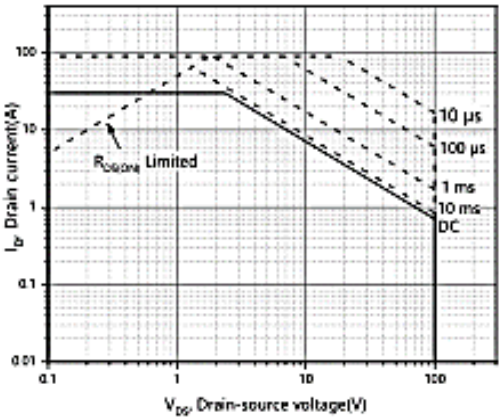
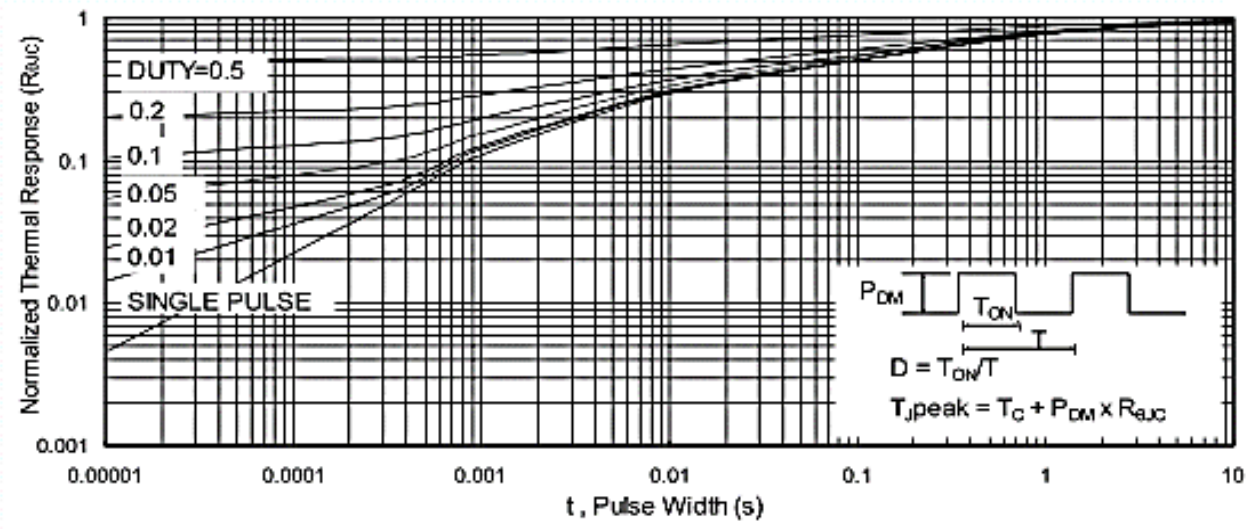
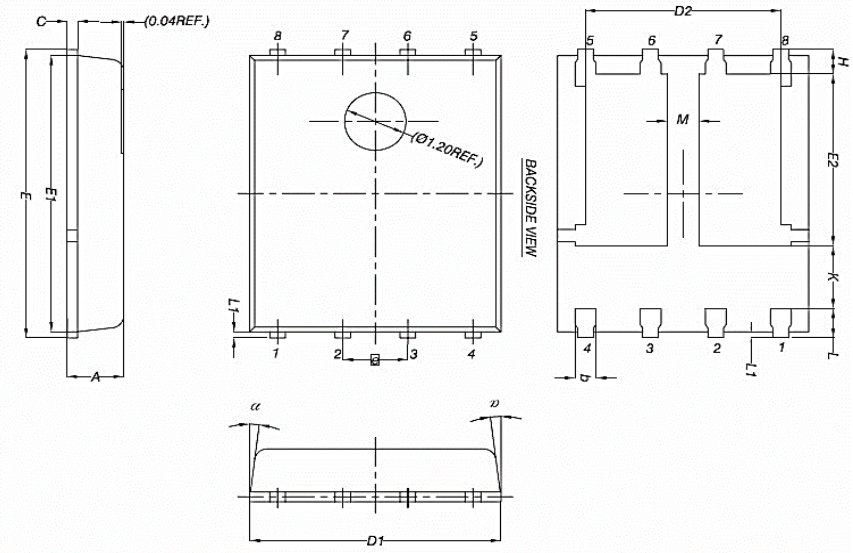



Figure 10, Safe operation area $T_C$=25 ℃




**Figu11. Normalized Maximum Transient Thermal Impedance**

## Package Mechanical Data-DFN5*6-8L-JQ Double




| Symbol | Common | | |
|---|---|---|---|
| | mm | | |
| | Mim | Nom | Max |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| C | 0.20 | 0.25 | 0.30 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 3.96 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 3.30 | 3.45 |
| E2 | 3.38 | 3.05 | 3.20 |
| e | 1.27BSC | | |
| H | 0.41 | 0.51 | 0.61 |
| K | 1.10 | -- | -- |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| M | 0.50 | -- | -- |
| a | 0° | -- | 12° |

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## 100V N+N-Channel Enhancement Mode MOSFET

| Edition | Date | Change |
|---|---|---|
| Rve1.0 | 2021/9/10 | Initial release |