NIKO-SEM

Dual P-Channel Logic Level Enhancement Mode Field Effect Transistor

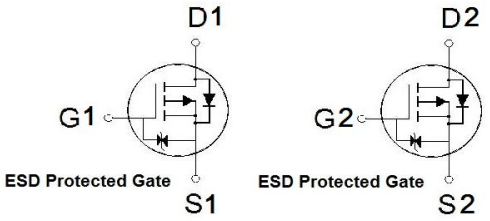
PZ567JZ

SOT-363

Halogen-Free & Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	520mΩ	-0.53A

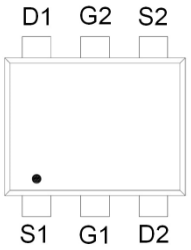


Features

- Pb−Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- ESD Protection − HBM Class : 1C.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.
- Space Limit & Smart Devices Applications.



G: GATE
D: DRAIN
S: SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current[1]	T_A = 25 °C	I_D	-0.53	A
	T_A = 70 °C		-0.42	
Pulsed Drain Current[2]		I_{DM}	-1	A
Power Dissipation	T_A = 25 °C	P_D	0.25	W
	T_A = 70 °C		0.16	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		500	°C / W

[1]Limited by maximum junction temperature.
[2]Limited by package.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

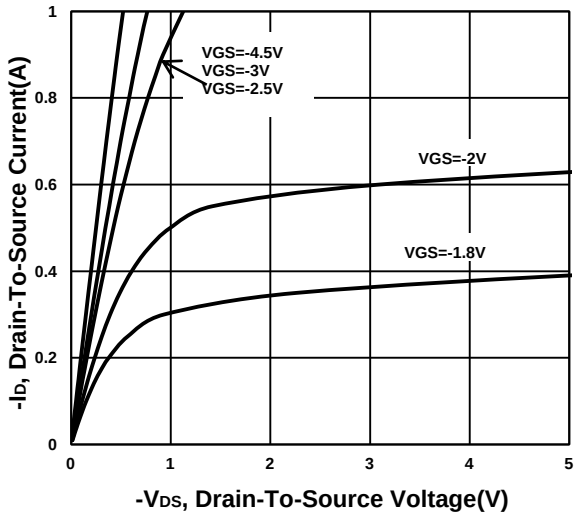
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-0.4	-0.96	-1.2	

Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±10V			±30	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	μA
		V_{DS} = -10V, V_{GS} = 0V, T_J = 125 °C			-10	
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -4.5V, I_D = -450mA		477	520	mΩ
		V_{GS} = -2.5V, I_D = -100mA		700	800	
		V_{GS} = -1.8V, I_D = -100mA		1200	3500	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -100mA		1.6		S

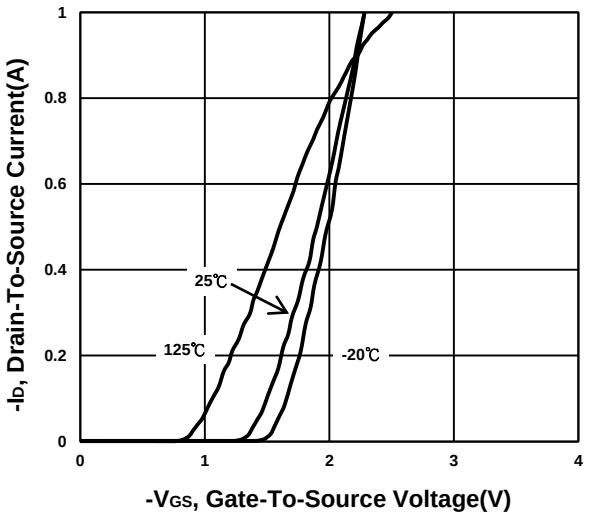
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -10V, f = 1MHz		48		pF
Output Capacitance	C_{oss}			18		
Reverse Transfer Capacitance	C_{rss}			10		
Total Gate Charge[2]	Q_g	V_{GS} = -4.5V , V_{DS} =-20V, I_D = -1A		1.1		nC
Gate-Source Charge[2]	Q_{gs}			0.2		
Gate-Drain Charge[2]	Q_{gd}			0.3		
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = -10V , $I_D \cong$ -450mA , V_{GS} = -4.5V, R_{GEN} = 5.1Ω		17		nS
Rise Time[2]	t_r			30		
Turn-Off Delay Time[2]	$t_{d(off)}$			76		
Fall Time[2]	t_f			46		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I_S				-0.2	A
Forward Voltage[1]	V_{SD}	I_F = -450mA, V_{GS} = 0V			-1.2	V
Reverse Recovery Time	t_{rr}	I_F = -1A, dI/dt = 100 A/μs		46		nS
Reverse Recovery Charge	Q_{rr}			28		nC

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.

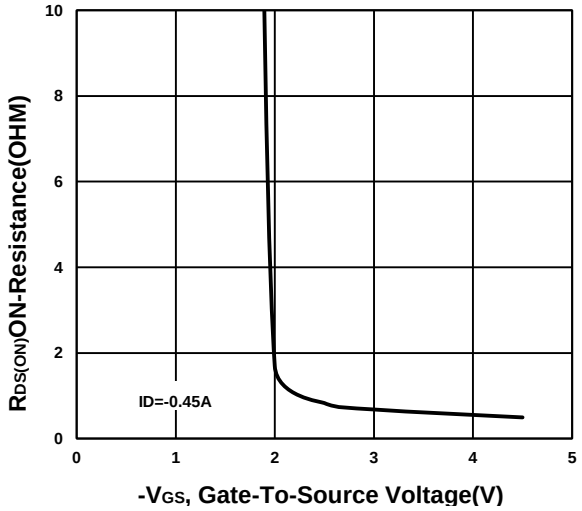
Output Characteristics



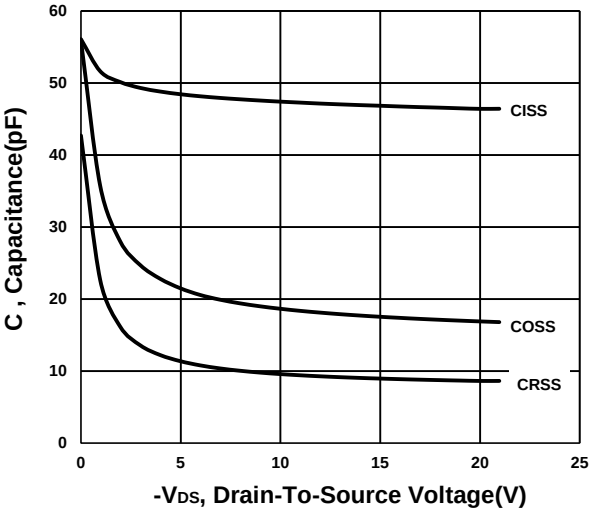
Transfer Characteristics



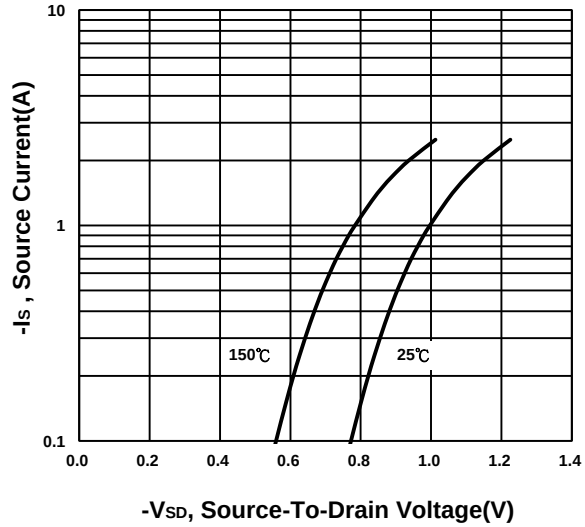
On-Resistance VS Gate-To-Source



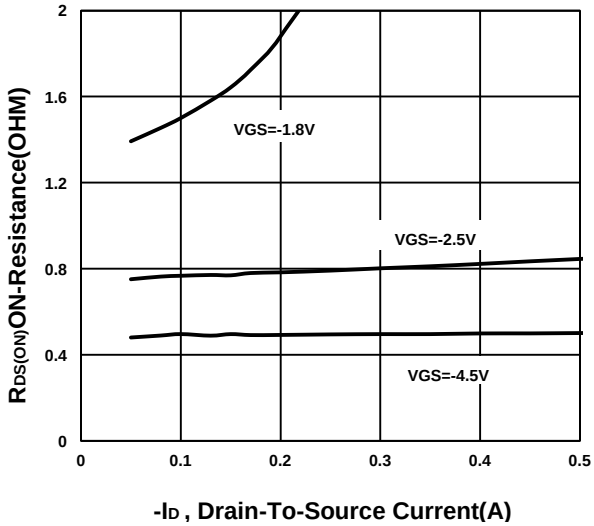
Capacitance Characteristic



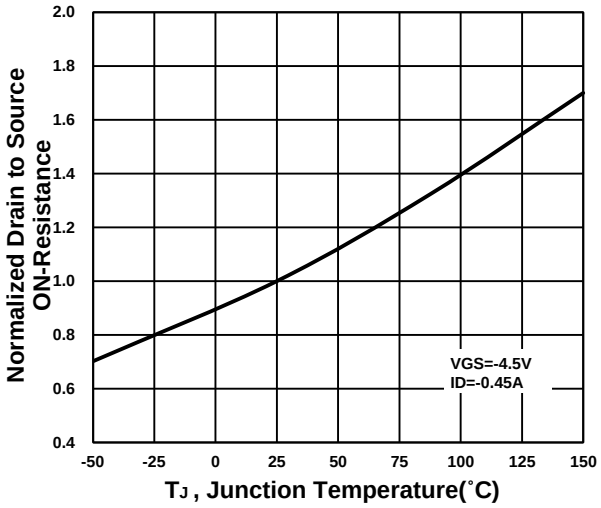
Source-Drain Diode Forward Voltage



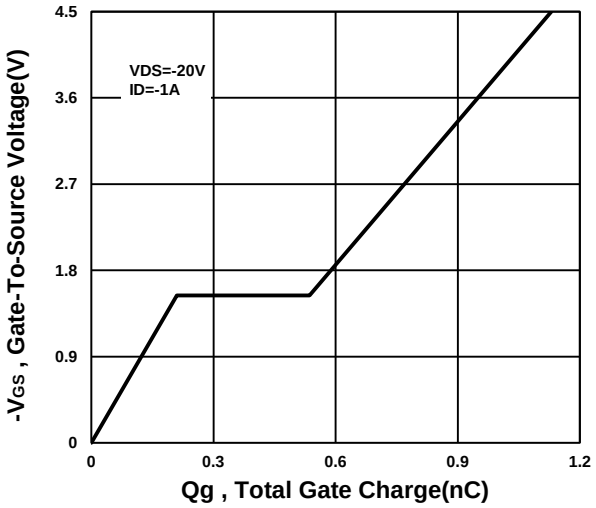
On-Resistance VS Drain Current



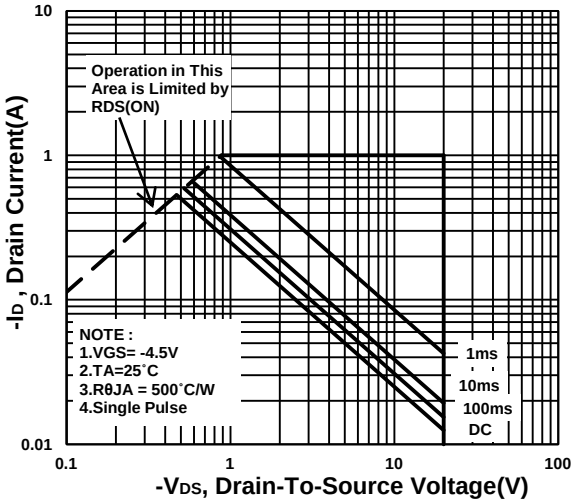
On-Resistance VS Temperature



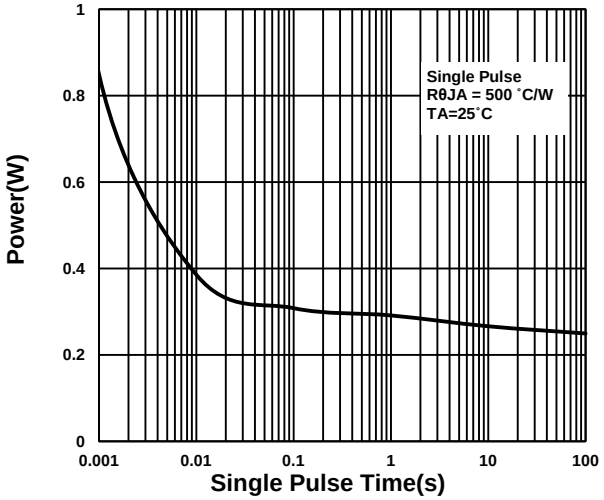
Gate charge Characteristics



Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve