

Features

- 100V/80A,
 $R_{DS(ON)} = 11m\Omega(Typ.)@V_{GS}=10V$
- Low $R_{DS(ON)}$
- Super High Dense Cell Design
- Spike Optimized Process
- 100% Avalanche Tested

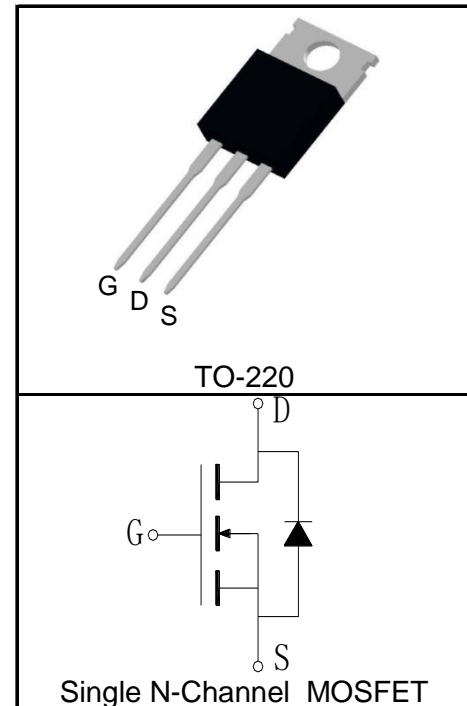
Applications

- Synchronous Rectification
- Power Management



Halogen-Free

Pin Description



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Common Ratings ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	175	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ\text{C}$
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$ 80	A
Mounted on Large Heat Sink			
$I_{DP}^{①}$	300 μs Pulse Drain Current Tested	$T_C=25^\circ\text{C}$ 320	A
$I_D^{②}$	Continuous Drain Current($V_{GS}=10V$)	$T_C=25^\circ\text{C}$ 80	A
		$T_C=100^\circ\text{C}$ 57	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ 150	W
		$T_C=100^\circ\text{C}$ 75	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^{③}$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C}/\text{W}$
Drain-Source Avalanche Ratings			
$E_{AS}^{④}$	Avalanche Energy, Single Pulsed	225	mJ

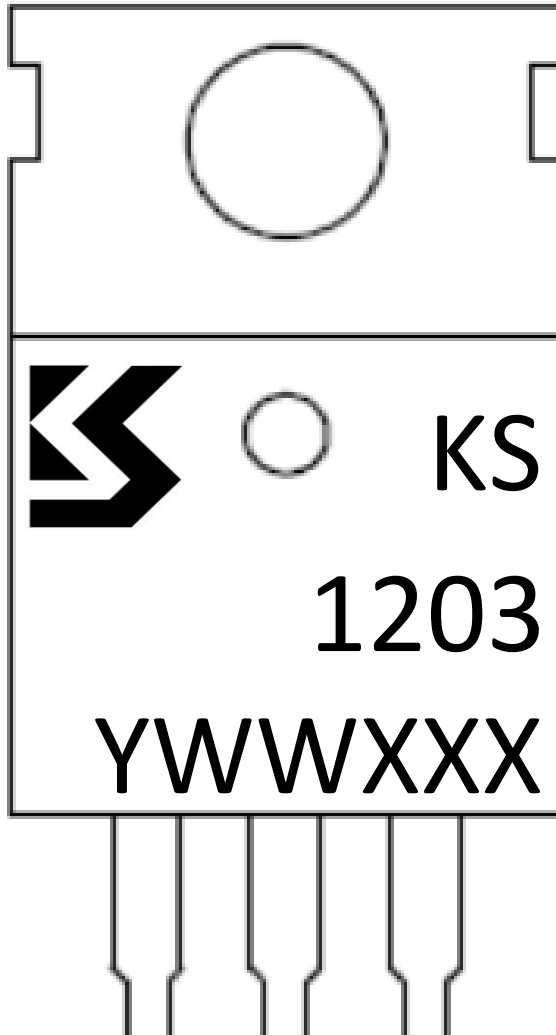
Electrical Characteristics ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	KS1203CB			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	100			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$			1	μA
		$T_J=125^\circ\text{C}$			30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	2.5	3.5	4.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
$R_{DS(ON)}^{(5)}$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=20A$		11	14	m Ω
Diode Characteristics						
$V_{SD}^{(5)}$	Diode Forward Voltage	$I_{SD}=20A, V_{GS}=0V$		0.81	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD}=20A, dI_{SD}/dt=100A/\mu s$		31		ns
Q_{rr}	Reverse Recovery Charge			55		nC
Dynamic Characteristics⁽⁶⁾						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$		1.3		Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=50V,$ Frequency=1.0MHz		3000		pF
C_{oss}	Output Capacitance			405		
C_{riss}	Reverse Transfer Capacitance			180		
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=50V, I_{DS}=20A,$ $V_{GEN}=10V, R_G=3\Omega$		13		ns
t_r	Turn-on Rise Time			16		
$t_{d(OFF)}$	Turn-off Delay Time			31		
t_f	Turn-off Fall Time			15		
Gate Charge Characteristics⁽⁶⁾						
Q_g	Total Gate Charge	$V_{DS}=50V, V_{GS}=10V,$ $I_{DS}=20A$		50		nC
Q_{gs}	Gate-Source Charge			14		
Q_{gd}	Gate-Drain Charge			19		

- Notes:
- ① Pulse width limited by safe operating area.
 - ② Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 75A.
 - ③ When mounted on 1 inch square copper board, $t \leq 10\text{sec}$. The value in any given application depends on the user's specific board design.
 - ④ Limited by $T_{Jmax}, I_{AS}=30A, L=0.5\text{mH}, V_{DD}=48V, R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.
 - ⑤ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 - ⑥ Guaranteed by design, not subject to production testing.

Ordering and Marking Information

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS1203CB	TO-220	Tube	50	-	-

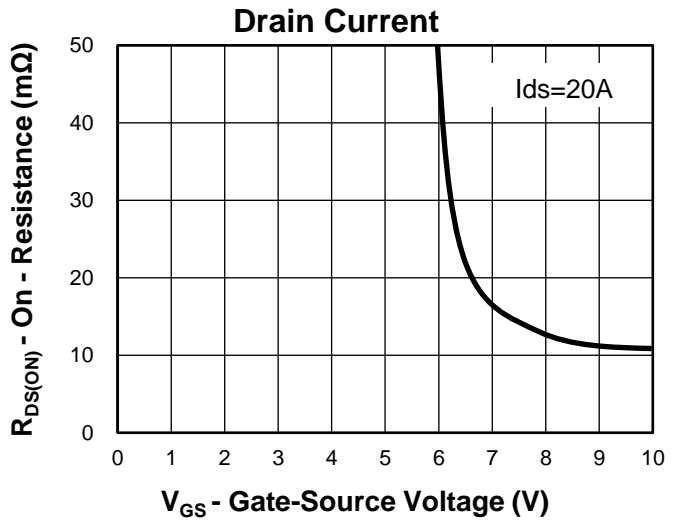
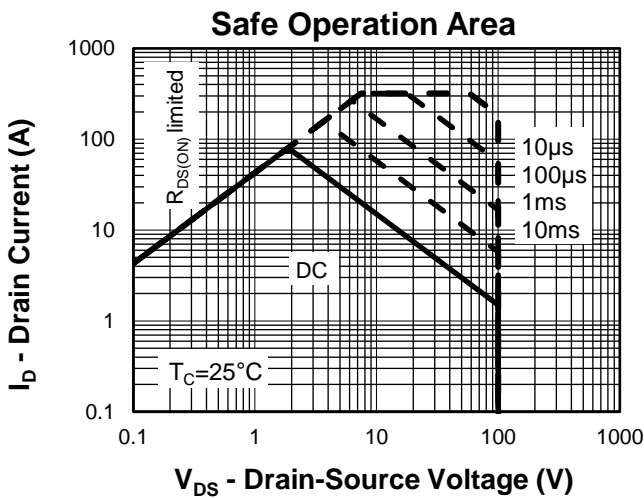
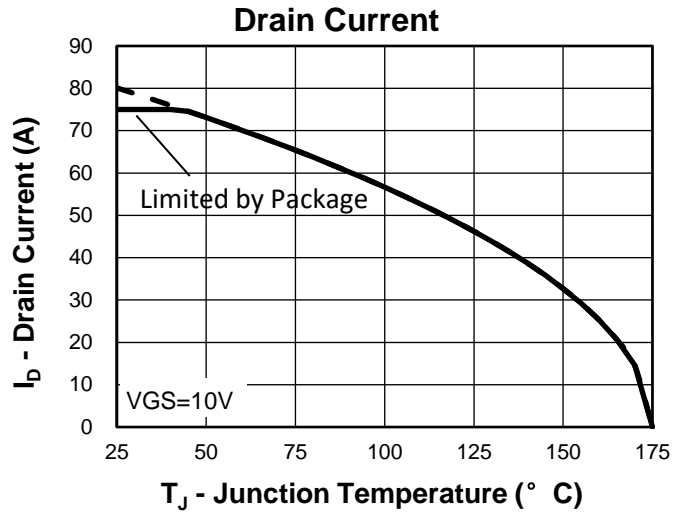
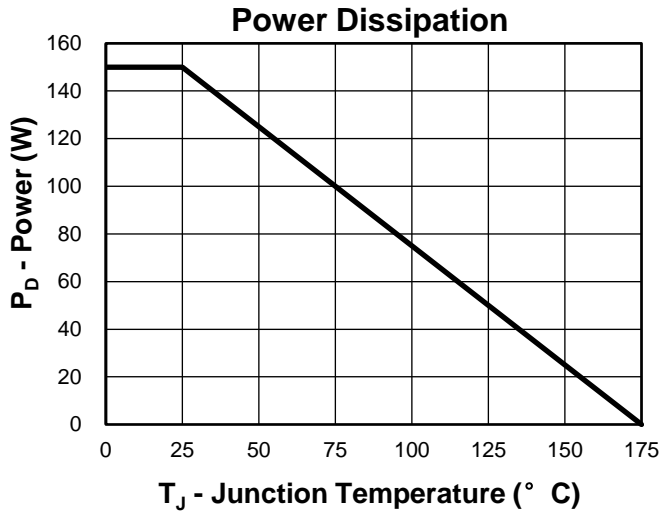


Y =Year,2017-A,2018-B,etc.

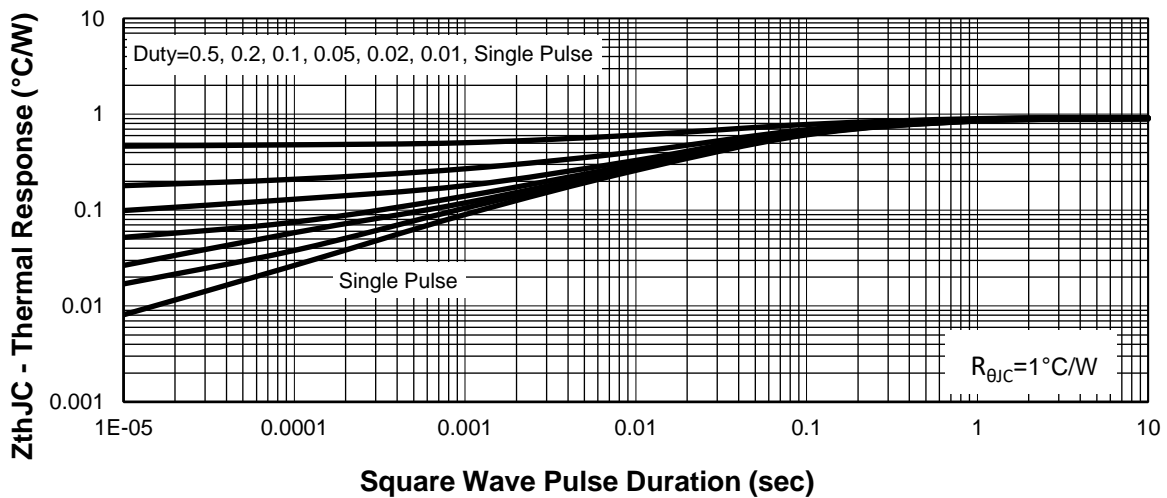
WW =Week.

XXX =Lot number.

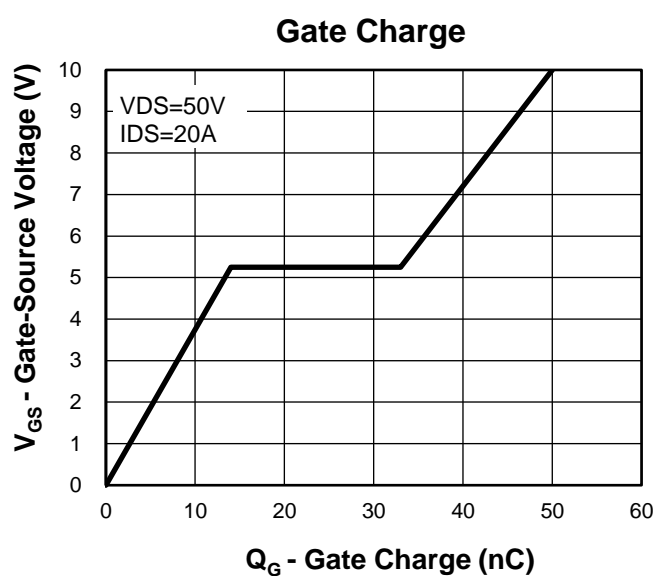
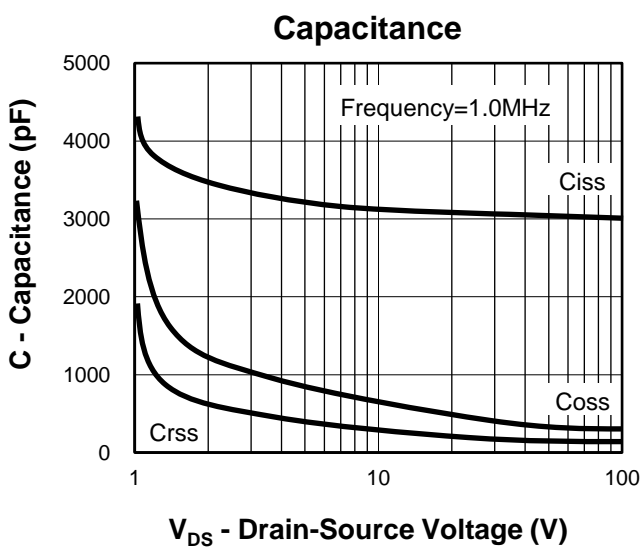
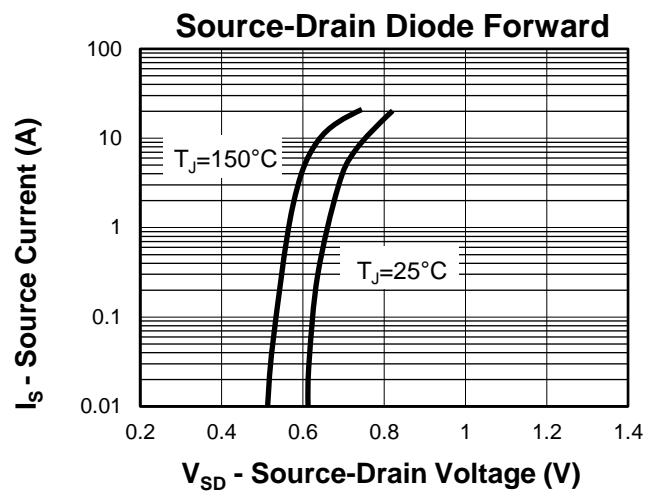
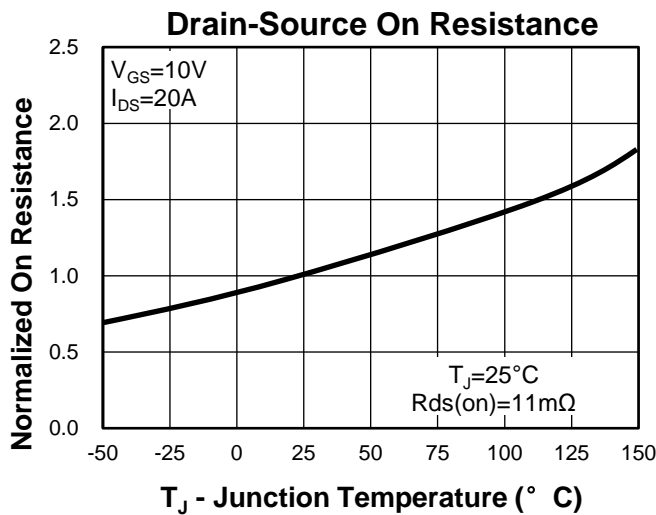
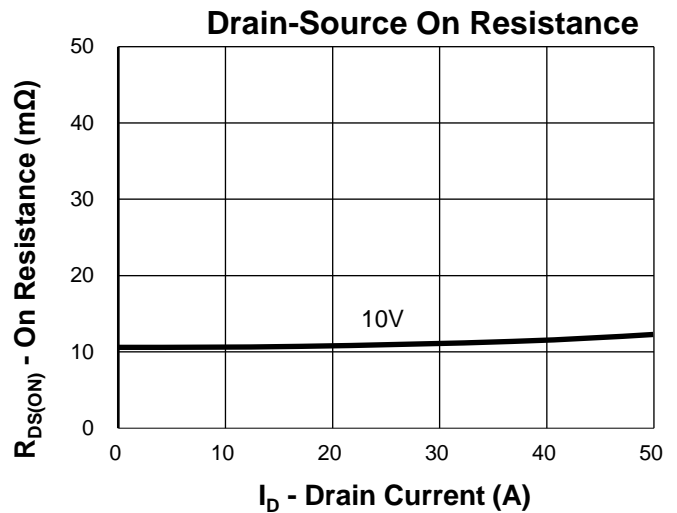
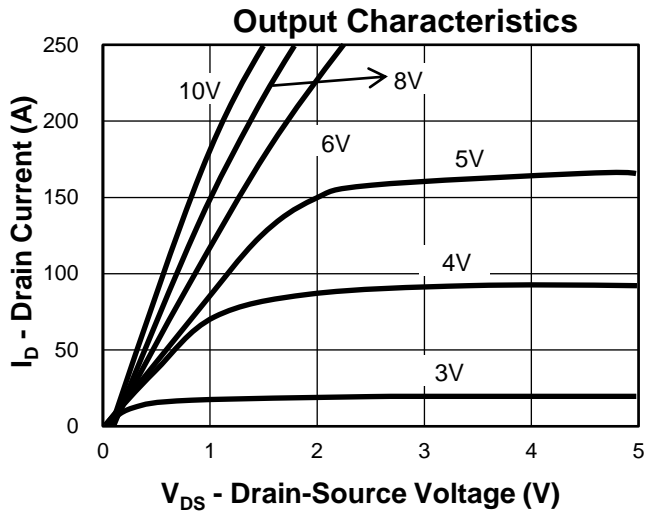
Typical Characteristics

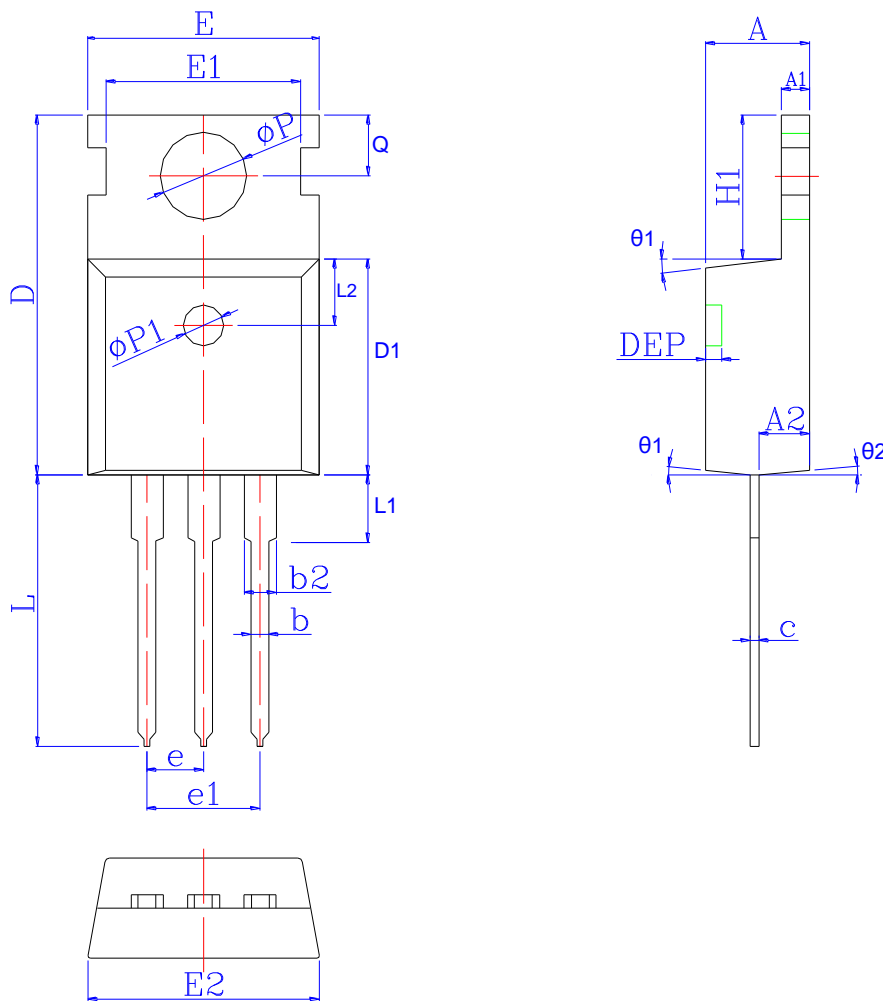


Thermal Transient Impedance



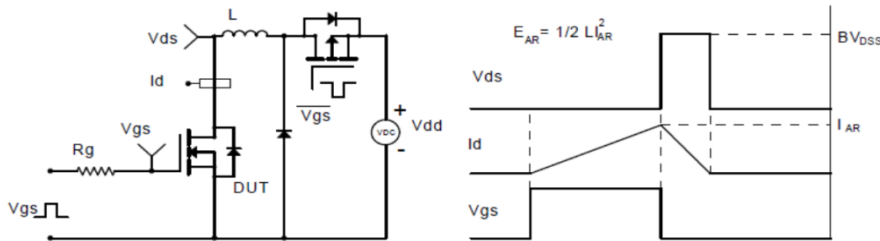
Typical Characteristics



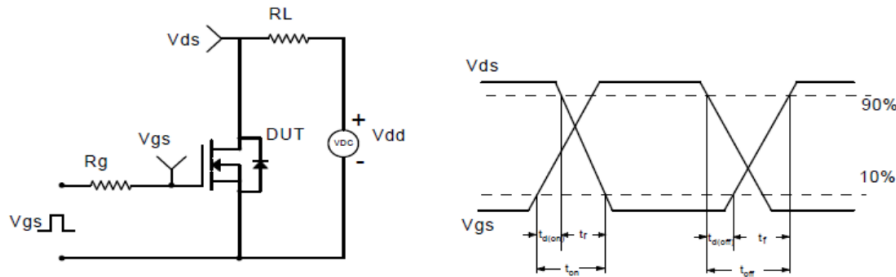
Package Information
TO-220


SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.54	4.77	0.169	0.179	0.188	Φp1	1.40	1.50	1.60	0.055	0.059	0.063
A1	1.15	1.30	1.40	0.045	0.051	0.055	e	2.54 BSC			0.10 BSC		
A2	1.90	2.25	2.60	0.075	0.089	0.102	e1	5.08 BSC			0.20 BSC		
b	0.60	0.80	1.00	0.024	0.031	0.039	H1	6.30	6.50	6.80	0.248	0.256	0.268
b2	1.17	1.28	1.72	0.046	0.050	0.068	L	12.70	13.18	13.65	0.500	0.519	0.537
c	0.40	0.50	0.60	0.016	0.020	0.024	L1	*	*	3.95	*	*	0.156
D	15.40	15.70	16.00	0.606	0.618	0.630	L2	2.50 REF			0.098 REF		
D1	8.96	9.21	9.46	0.353	0.363	0.372	Φp	3.50	3.60	3.75	0.138	0.142	0.148
DEP	*	*	0.30	*	*	0.012	Q	2.70	2.80	3.20	0.106	0.110	0.126
E	9.66	9.97	10.28	0.380	0.393	0.405	θ1	5°	7°	9°	5°	7°	9°
E1	*	8.70	*	*	0.343	*	θ2	1°	3°	5°	1°	3°	5°
E2	9.80	10.00	10.20	0.386	0.394	0.402							

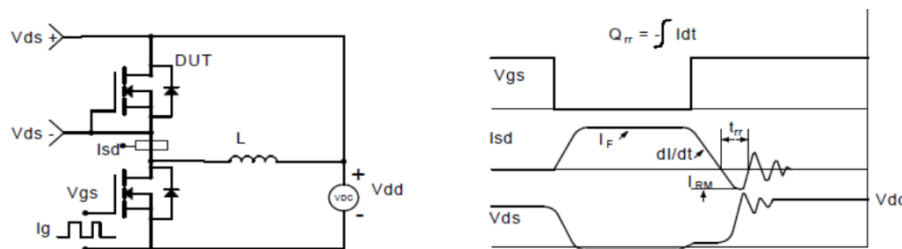
Avalanche Test Circuit and Waveforms



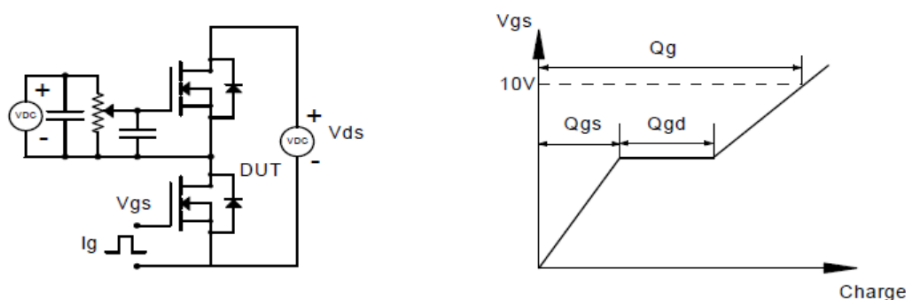
Switching Time Test Circuit and Waveforms



Diode Recovery Test Circuit and Waveforms



Gate Charge Test Circuit and Waveform



Customer Service

Kwansemi Semiconductor Co.,Ltd

Email:Sales@kwansemi.com

Web:www.kwansemi.com

DISCLAIMER:

Kwansemi reserves the right to change the specifications and circuitry without notice at any time. The Products are not designed for use in hostile environments, including, without limitation, aircraft, nuclear power generation, medical appliances, and devices or systems in which malfunction of any Product can reasonably be expected to result in a personal injury. Seller's customers using or selling Seller's products for use in such applications do so at their own risk and agree to fully defend and indemnify Seller.