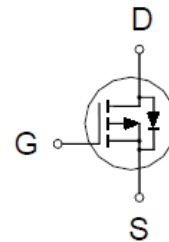
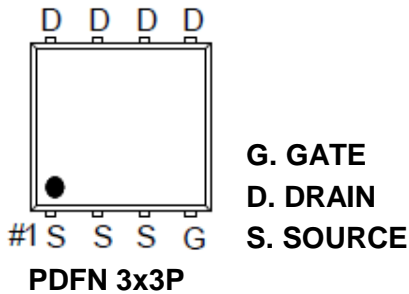


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P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-20V	6.5m Ω @ $V_{GS} = -4.5V$	-43A



100% UIS Tested
100% Rg Tested

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ⁴	$T_C = 25\text{ }^\circ\text{C}$	I_D	-43	A
	$T_C = 100\text{ }^\circ\text{C}$		-27	
	$T_A = 25\text{ }^\circ\text{C}$		-18	
	$T_A = 70\text{ }^\circ\text{C}$		-14	
Pulsed Drain Current ¹		I_{DM}	-50	
Avalanche Current		I_{AS}	-39	
Avalanche Energy	L = 0.1mH	E_{AS}	76	mJ
Power Dissipation ³	$T_C = 25\text{ }^\circ\text{C}$	P_D	20	W
	$T_C = 100\text{ }^\circ\text{C}$		8	
	$T_A = 25\text{ }^\circ\text{C}$		3.5	
	$T_A = 70\text{ }^\circ\text{C}$		2.2	
Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE		SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$t \leq 10s$	$R_{\theta JA}$		35	°C / W
Junction-to-Ambient ²	Steady-State	$R_{\theta JA}$		60	
Junction-to-Case	Steady-State	$R_{\theta JC}$		6	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$.

³The Power dissipation is based on $R_{\theta JA}$ $t \leq 10s$ value.

⁴Package limitation current is 36A.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ C$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS		
			MIN	TYP	MAX			
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.45	-0.6	-0.9			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 8V$			± 100	nA		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16V, V_{GS} = 0V$			-1	μA		
		$V_{DS} = -10V, V_{GS} = 0V, T_J = 55^\circ C$			-10			
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -3.5A$		4.9	6.5	m Ω		
		$V_{GS} = -2.5V, I_D = -3.5A$		6	8			
		$V_{GS} = -1.8V, I_D = -2A$		7.6	11			
Forward Transconductance ¹	g_{fs}	$V_{DS} = -10V, I_D = -3.5A$		47		S		
DYNAMIC								
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		5926		pF		
Output Capacitance	C_{oss}			551				
Reverse Transfer Capacitance	C_{rss}			424				
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$		4		Ω		
Total Gate Charge ²	$Q_g(V_{GS}=-4.5V)$	$V_{DS} = -10V, I_D = -3.5A$		64		nC		
	$Q_g(V_{GS}=-2.5V)$			38				
Gate-Source Charge ²	Q_{gs}			6.7				
Gate-Drain Charge ²	Q_{gd}			12.7				
Turn-On Delay Time ²	$t_{d(on)}$		$V_{DD} = -10V, I_D \cong -3.5A, V_{GS} = -4.5V, R_{GEN} = 6\Omega$		35			nS
Rise Time ²	t_r				53			
Turn-Off Delay Time ²	$t_{d(off)}$			190				
Fall Time ²	t_f			109				

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)

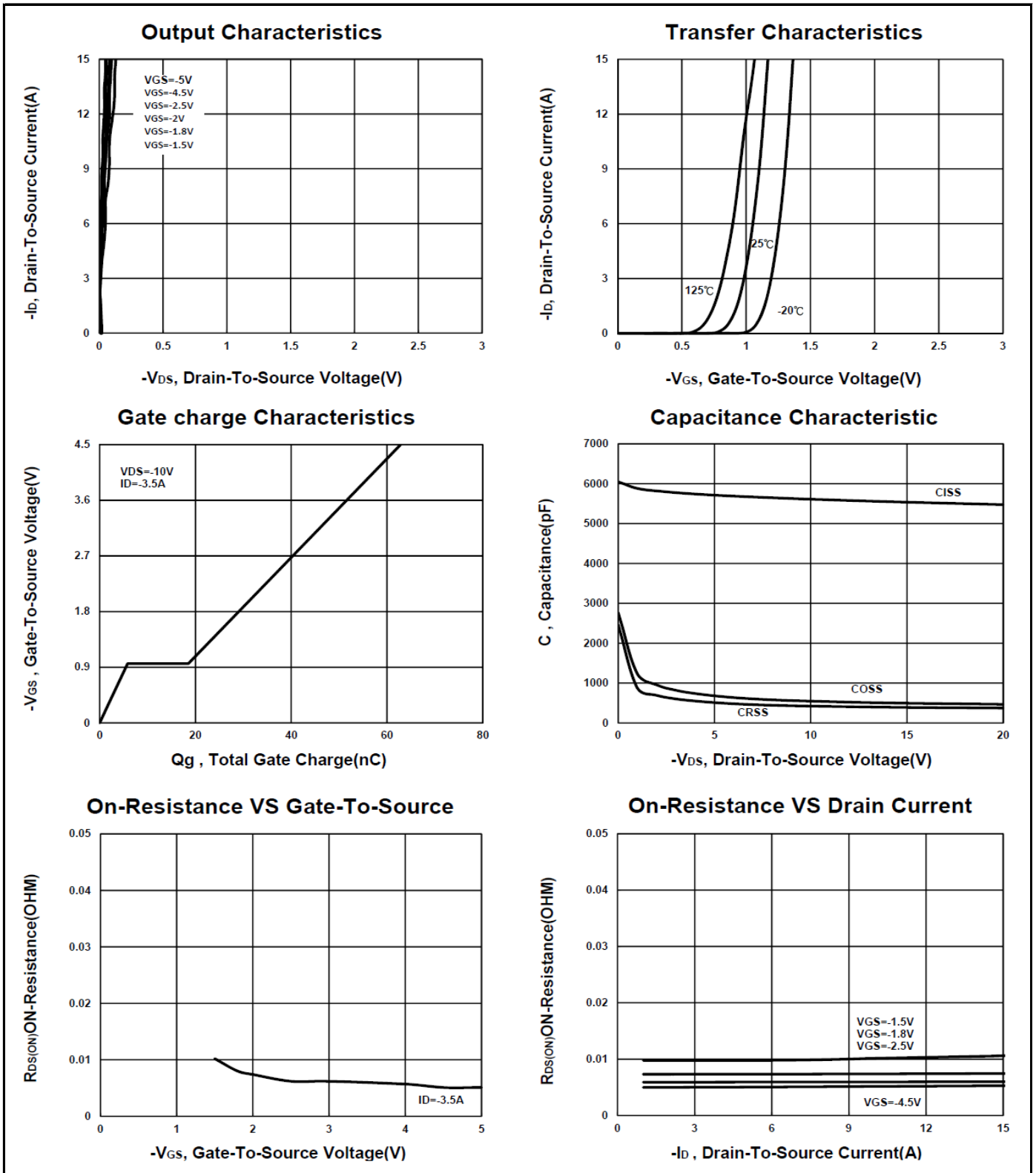
Continuous Current	I _S			-15	A
Forward Voltage ¹	V _{SD}	I _F = -3.5A, V _{GS} = 0V		-1.3	V
Reverse Recovery Time	t _{rr}	I _F = -3.5A, di/dt = 100A / μS		37	nS
Reverse Recovery Charge	Q _{rr}			26	nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

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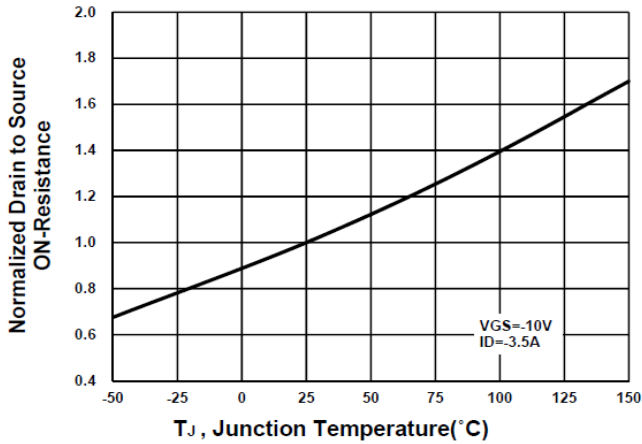
P-Channel Logic Level Enhancement Mode MOSFET



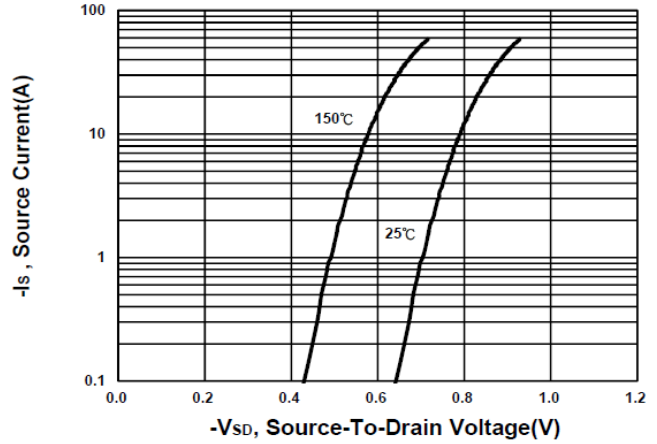
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P-Channel Logic Level Enhancement Mode MOSFET

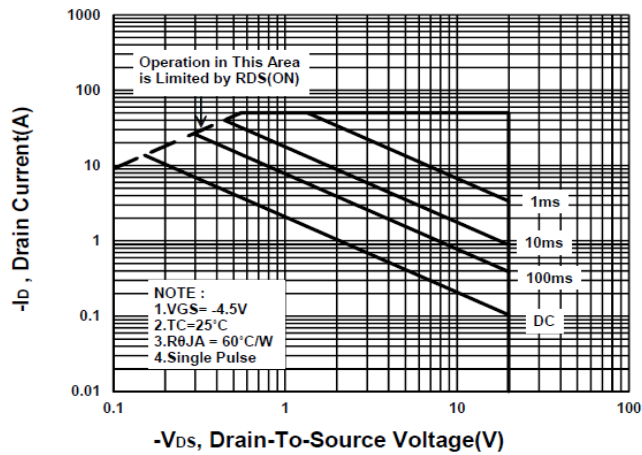
On-Resistance VS Temperature



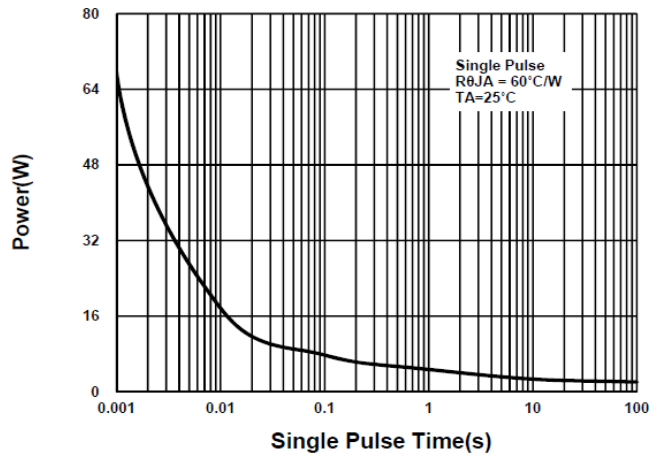
Source-Drain Diode Forward Voltage



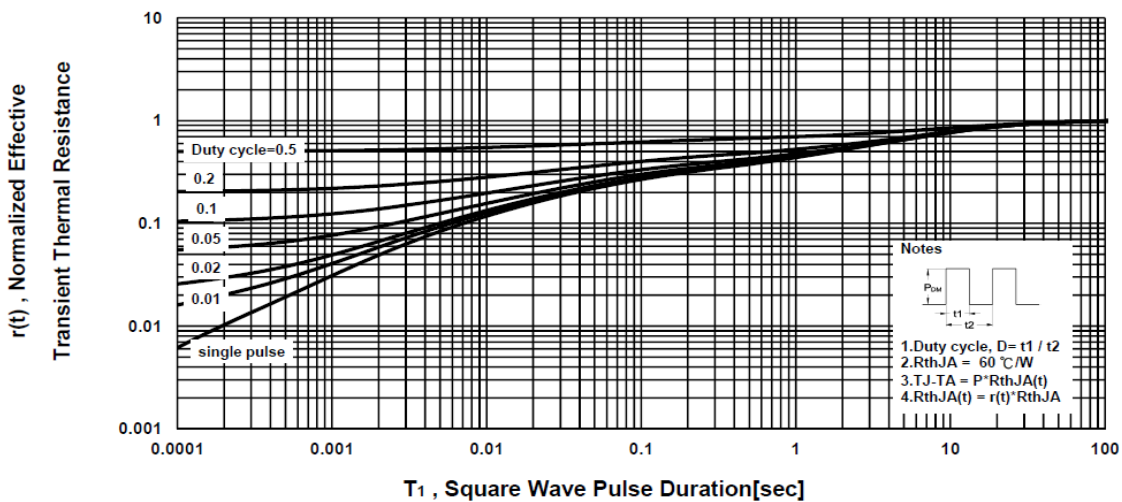
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



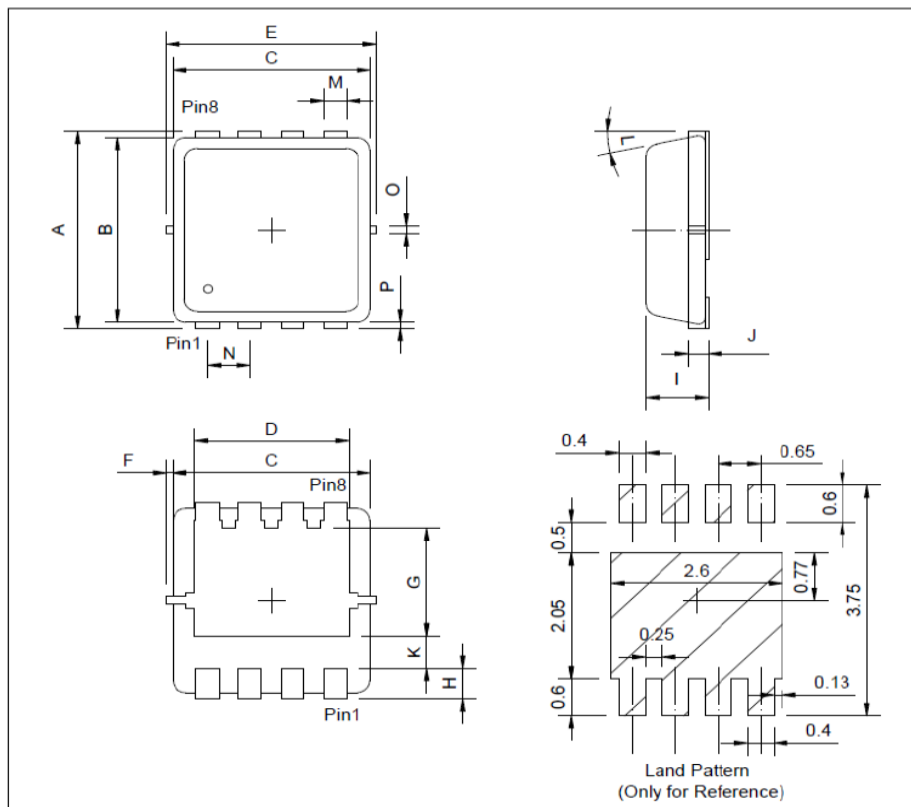
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Package Dimension

PDFN 3x3P MECHANICAL DATA

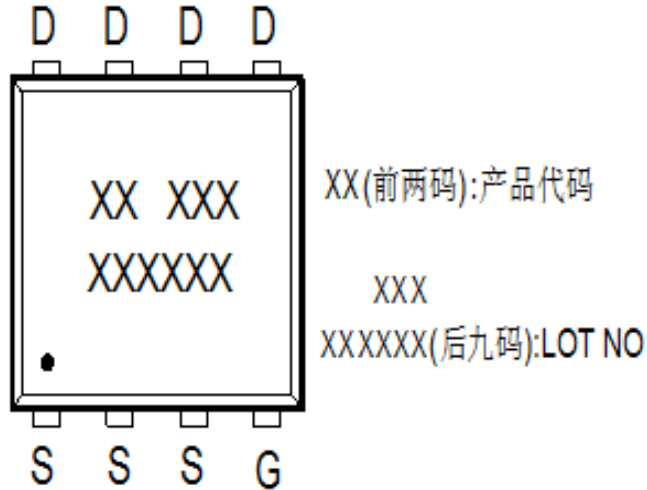
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	3	3.3	3.6	I	0.65	0.8	0.9
B	2.88	3	3.2	J	0.1	0.15	0.25
C	2.9	3	3.25	K	0.59		
D	2.29	2.45	2.69	L	0°	10°	12°
E	3	3.3	3.6	M	0.14	0.3	0.4
F	0	0.1	0.2	N	0.55	0.65	0.75
G	1.35	1.75	2.2	O		0.2	
H	0.15	0.3	0.55	P	0		0.2



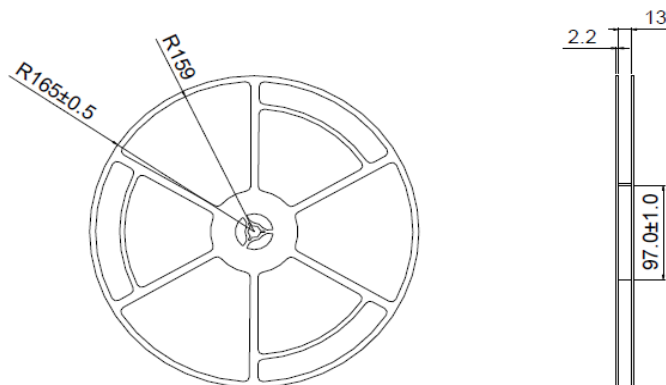
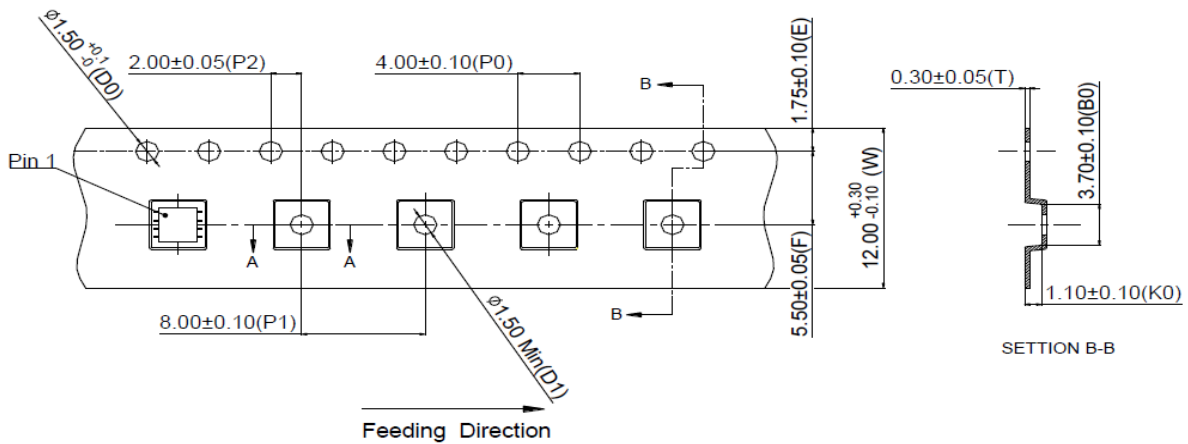
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A. Marking Information(此产品代码为: L7)



B. Tape & Reel Information: 5000pcs/Reel

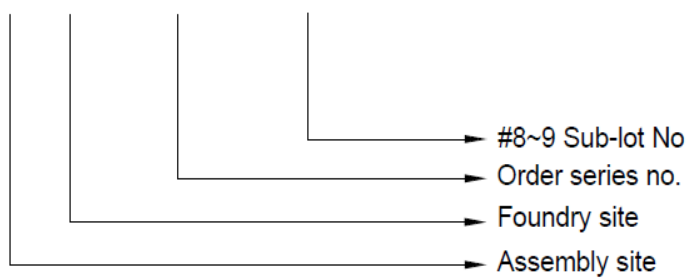


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C. Lot.No. & Date Code rule

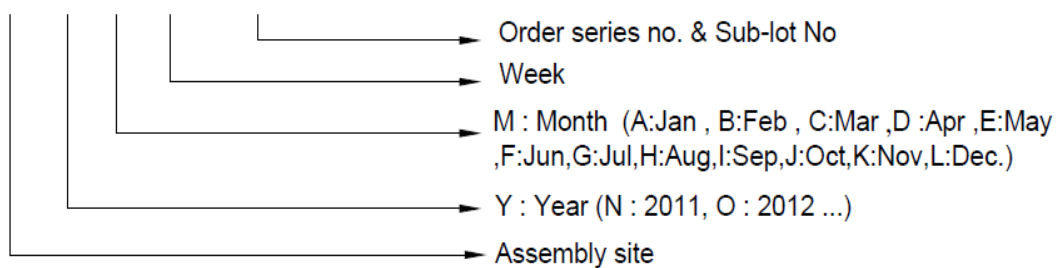
1.LOT.NO.

M N 15M21 03



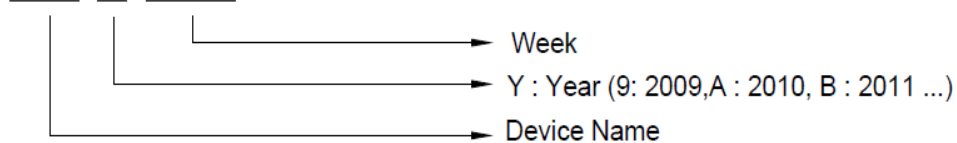
2.Date Code

D Y M X XXX



3.Date Code (for Small package)

XX Y WW





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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文”0”和数字”0”，”G和”Q”的字型即可)
3	Great Power	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	Pb Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 1 cm bottom color: Green Font color: Black Font style: Arial
12	Scan info	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least