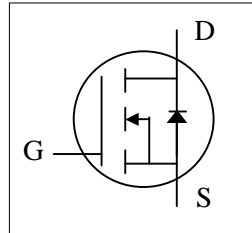




- ▼ Simple Drive Requirement
- ▼ Lower On-resistance
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant & Halogen-Free

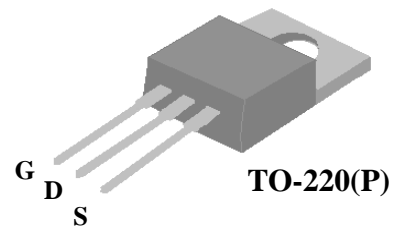


BV_{DSS}	75V
$R_{DS(ON)}$	8m Ω
I_D	80A

Description

AP94T07 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



Absolute Maximum Ratings @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	75	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_c=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^3$	80	A
$I_D @ T_c=100^\circ\text{C}$	Drain Current, $V_{GS} @ 10V$	58	A
I_{DM}	Pulsed Drain Current ¹	300	A
$P_D @ T_c=25^\circ\text{C}$	Total Power Dissipation	125	W
E_{AS}	Single Pulse Avalanche Energy ⁴	45	mJ
T_{STG}	Storage Temperature Range	-55 to 175	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 175	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Maximum Thermal Resistance, Junction-case	1.2	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$



AP94T07GP-HF

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	75	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=40A$	-	-	8	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	5	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=40A$	-	55	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=60V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Q_g	Total Gate Charge	$I_D=40A$	-	58	92	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=60V$	-	14	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	29	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{DS}=40V$	-	13	-	ns
t_r	Rise Time	$I_D=40A$	-	80	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=1\Omega, V_{GS}=10V$	-	26	-	ns
t_f	Fall Time	$R_D=1\Omega$	-	12	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	2350	3760	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	390	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	245	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.3	-	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=40A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_S=10A, V_{GS}=0V,$	-	46	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	83	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Package limitation current is 80A.
4. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=30V$, $L=0.1\text{mH}$, $R_G=25\Omega$, $I_{AS}=30A$.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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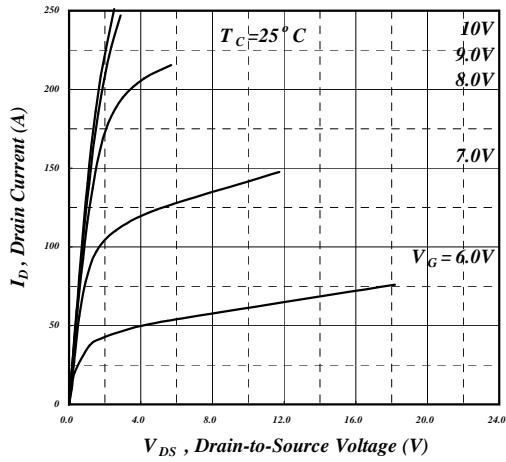


Fig 1. Typical Output Characteristics

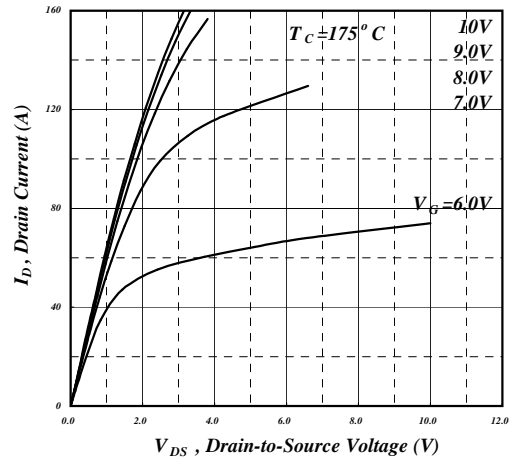


Fig 2. Typical Output Characteristics

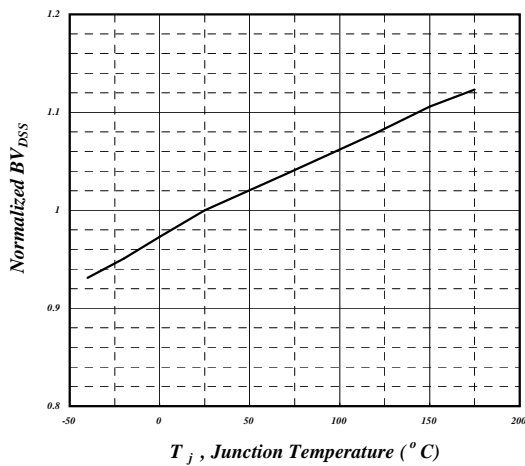


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

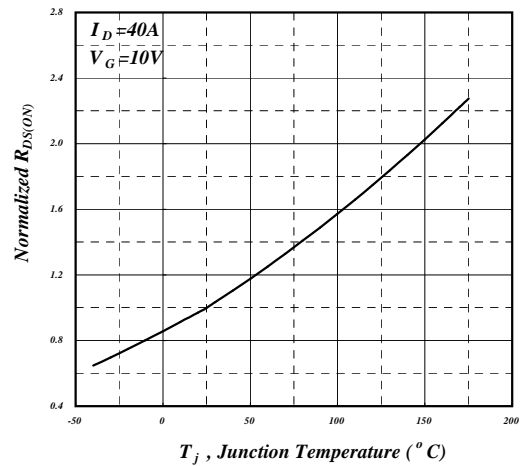


Fig 4. Normalized On-Resistance v.s. Junction Temperature

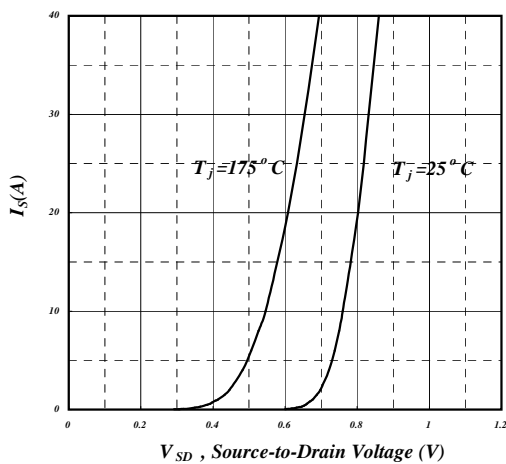


Fig 5. Forward Characteristic of Reverse Diode

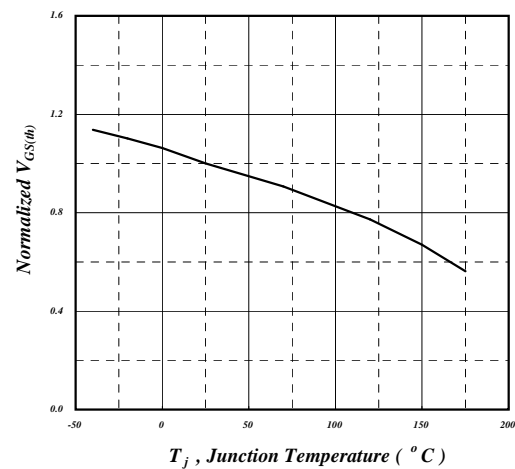


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

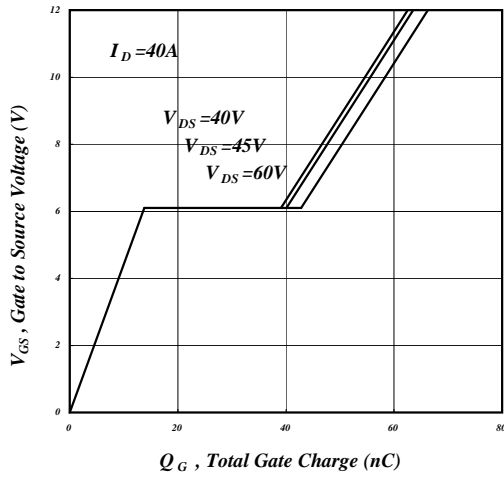


Fig 7. Gate Charge Characteristics

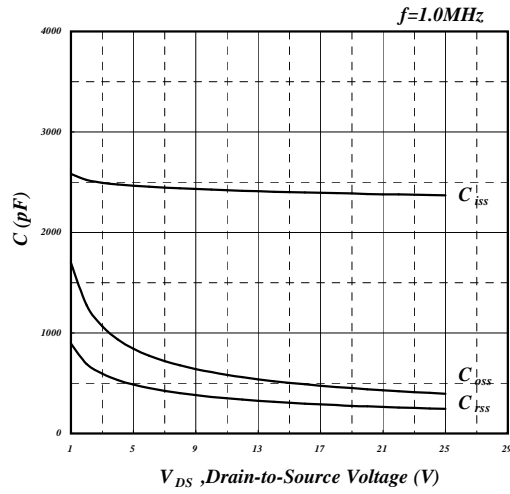


Fig 8. Typical Capacitance Characteristics

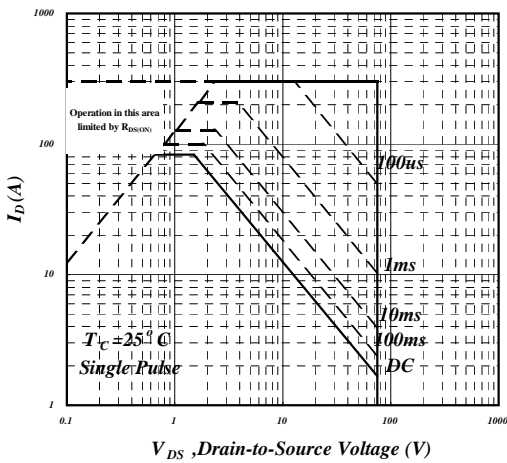


Fig 9. Maximum Safe Operating Area

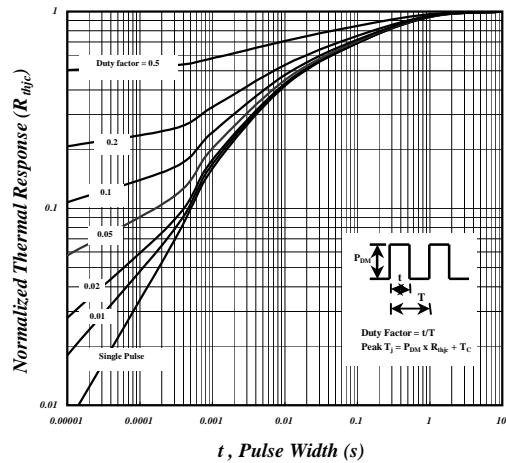


Fig 10. Effective Transient Thermal Impedance

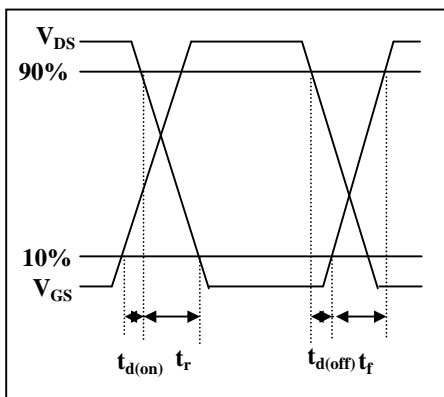


Fig 11. Switching Time Waveform

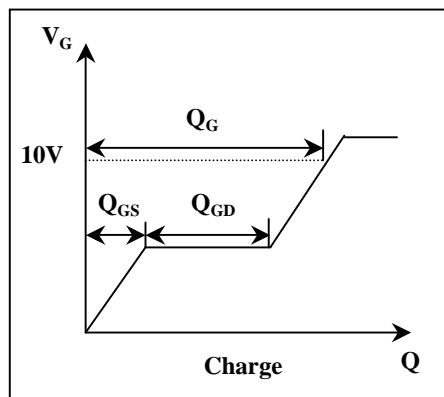


Fig 12. Gate Charge Waveform



MARKING INFORMATION

