Product Specification

GENERAL DESCRIPTION

DP2269 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to tight range. At no load or light load condition, the IC operates in extended burst mode to minimize switching loss, which can achieve less than 75mW standby.

VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with DP2269.

DP2269 offers comprehensive protections coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), on-chip Thermal Shutdown (OTP), VDD over voltage protection (VDD OVP) and VDD under voltage lockout (UVLO), etc. Excellent EMI performance is achieved with frequency shuffling and soft totem pole gate drive

The tone energy at below 20KHz is minimized in the design and audio noise is eliminated during operation.

DP2269 is offered in SOP8 package.

FEATURES

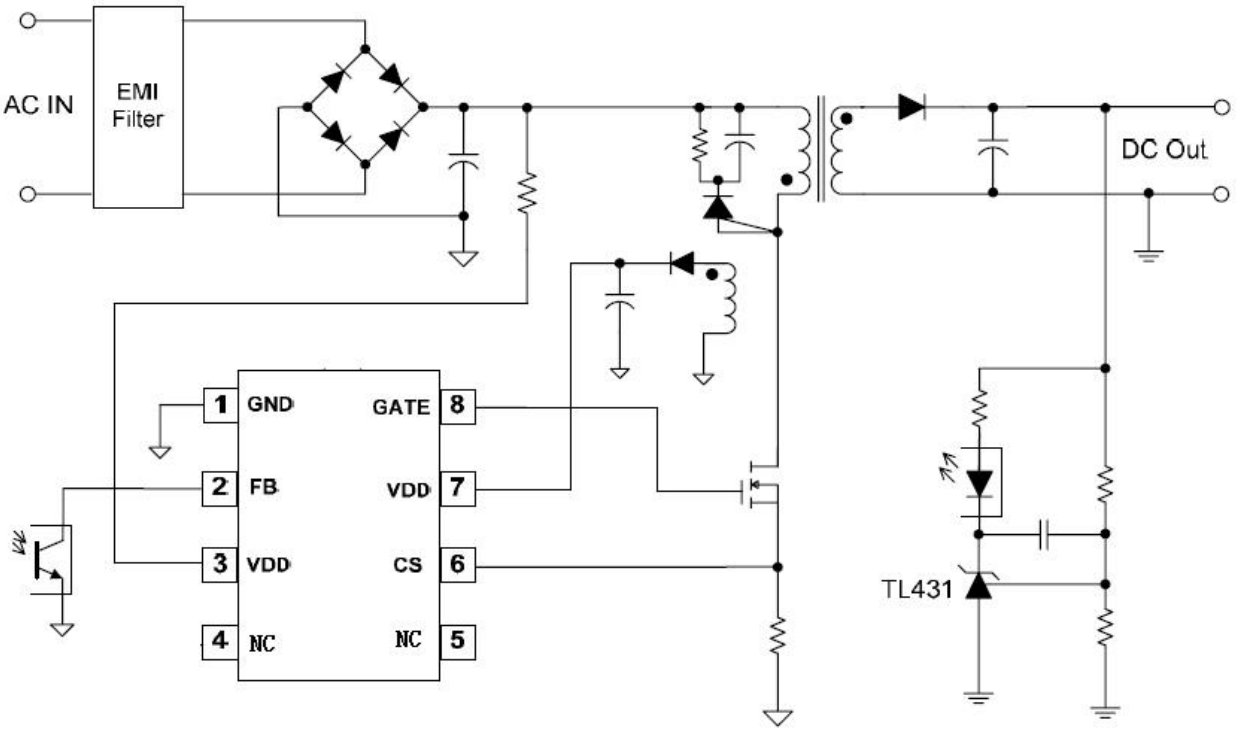
- Less than 75mW Standby Power at Universal Input
- Power on Soft Start Reducing MOSFET Vds Stress
- Frequency Shuffling for EMI
- Fixed 65KHz Switching Frequency
- Internal Synchronized Slope Compensation
- Low VDD Startup Current and Low Operating Current
- Built-in Leading Edge Blanking
- On-chip Thermal Shutdown
- Soft Gate Driver for Good EMI Performance
- Over Load Protection
- Cycle-by-Cycle Current Limiting
- VDD Under Voltage Lockout with Hysteresis (UVLO)
- VDD OVP & Clamp

APPLICATIONS

Offline AC/DC flyback converter for

- AC/DC Adapter
- Open-frame SMPS

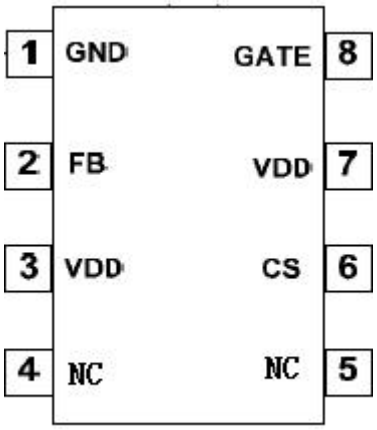
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of SOP8 package is shown as below.



Ordering Information

Part Number	Description
DP2269	SOP8, Pb free in T&R

Package Dissipation Rating

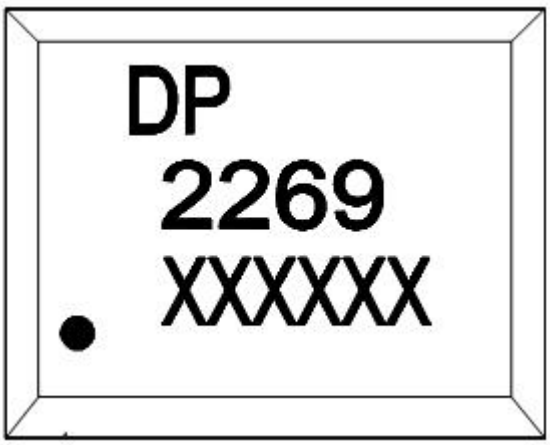
Package	RθJA (℃/W)
SOP8	150

Absolute Maximum Ratings

Parameter	Value
VDD Zener Clamp Voltage	V_{DD_Clamp}
VDD Clamp Continuous Current	10 mA
CS Input Voltage	-0.3 to 7V
FB Input Voltage	-0.3 to 7V
GATE Voltage Range	20V
Maximum Operating Junction Temperature T_J	150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Marking Information



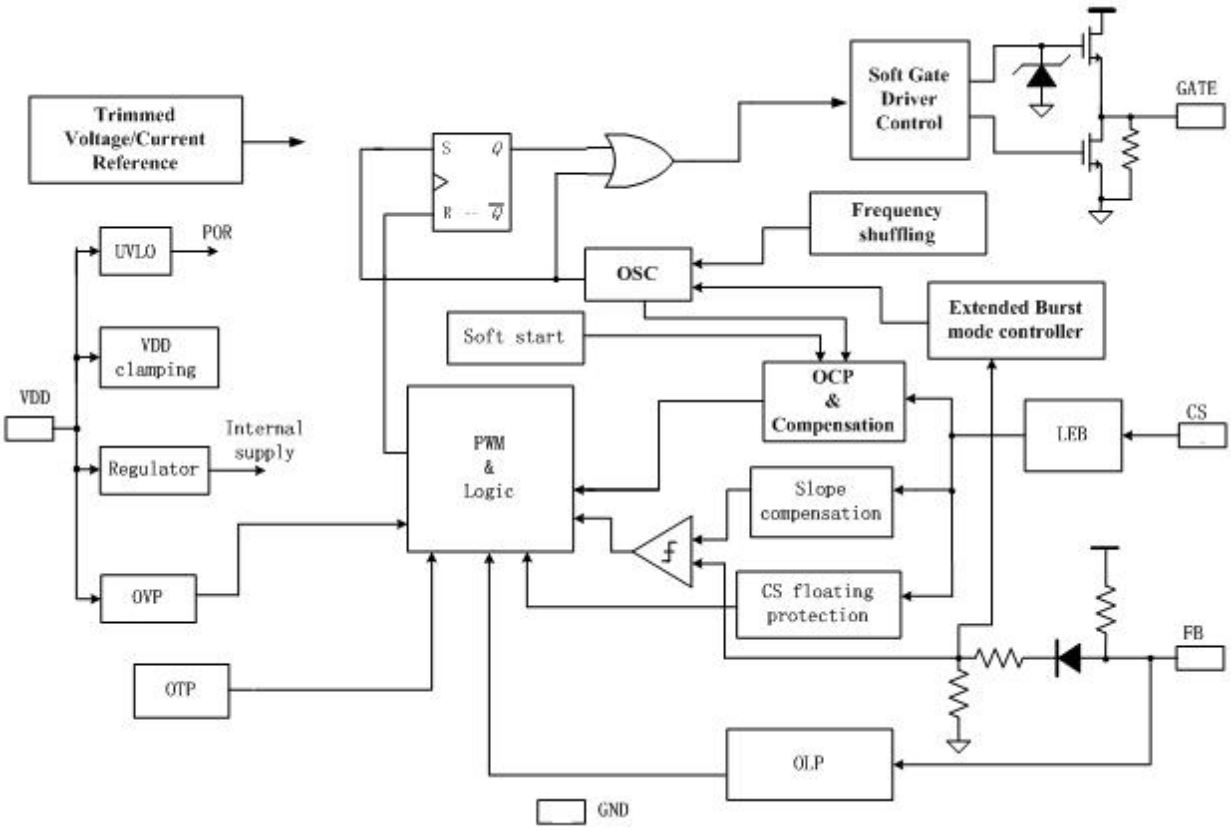
DP2269 for product name;

XXXXXX The first X reresents the last year,2014 is 4; The second X represents the month, in A-L 12 letters;The third and fourth X on behalf of the date, 01-31 said; The last two X represents the wafer batch code.

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground.
2	FB	I	Feedback pin. The loop regulation is achieved by connecting a photo-coupler to this pin. PWM duty cycle is determined by this pin voltage and the current sense signal at Pin 4.
3	VDD	P	Power supply.
4	NC	-	No connection.
5	NC	-	No connection.
6	CS	I	Current sense input.
7	VDD	P	Power supply.
8	GATE	O	Totem-pole gate driver output to drive the external MOSFET.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

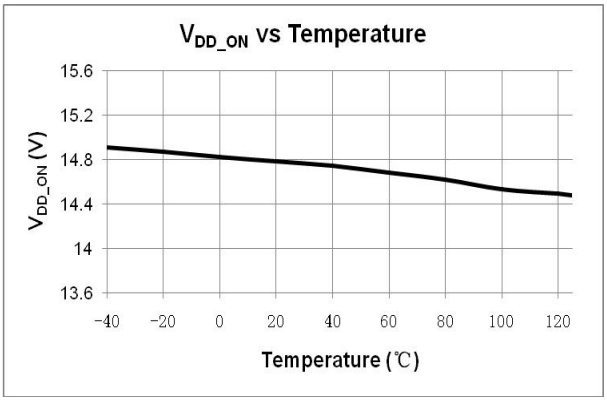
Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	11	26	V
T_A	Operating Ambient Temperature	-40	85	°C

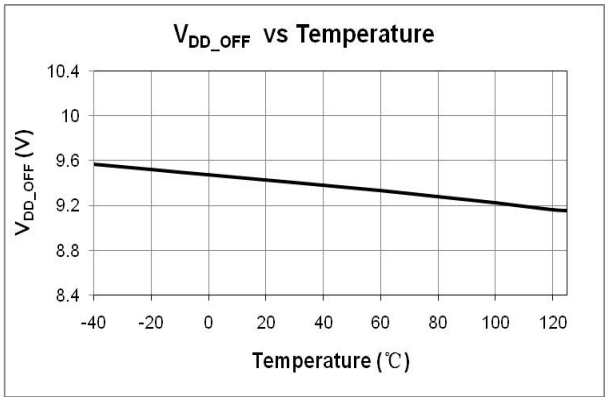
ELECTRICAL CHARACTERISTICS

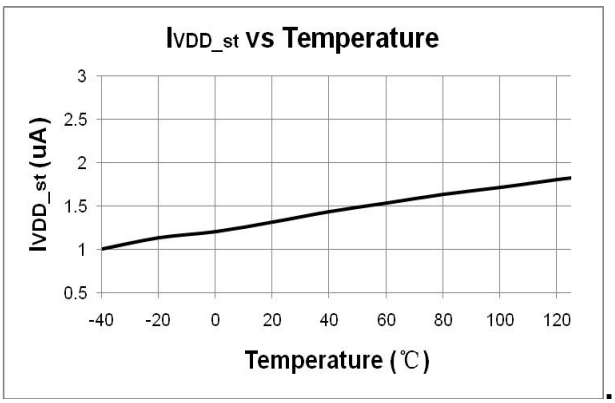
(T_A = 25°C, VDD=18V if not otherwise noted)

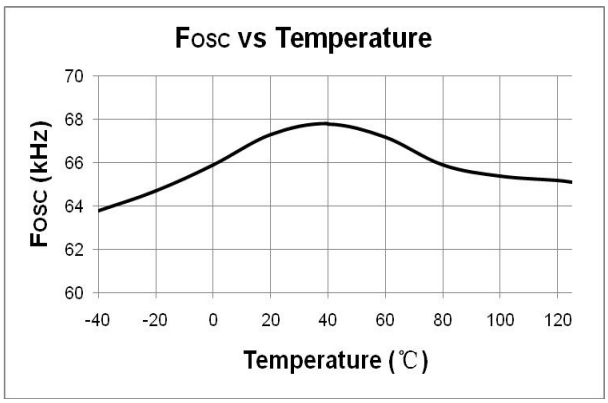
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section (VDD Pin)						
I_{VDD_st}	Start-up current into VDD pin			2	10	uA
I_{VDD_Op}	Operation Current	V_{FB}=3V,GATE=1nF		1.2	2	mA
$I_{VDD\_standby}$	Standby Current			0.4	1	mA
V_{DD_ON}	VDD Under Voltage Lockout Exit		13.5	14.5	15.5	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter		8.6	9.4	10.2	V
V_{DD_OVP}	VDD OVP Threshold		27	28.5	30	V
V_{DD_Clamp}	VDD Zener Clamp Voltage	$I(V_{DD})$ = 7 mA	30.5	32	33.5	V
Feedback Input Section (FB Pin)						
V_{FB_Open}	FB Open Voltage		4.5	5.4	6	V
I_{FB_Short}	FB Short Circuit Current	Short FB Pin to GND, Measure Current		0.3		mA
A_{CS}	PWM Gain	$\Delta V_{FB}/\Delta V_{CS}$		2.0		V/V
V_{skip}	FB Under Voltage GATE Clock is OFF			1.0		V
V_{TH_OLP}	Power Limiting FB Threshold Voltage			3.6		V
T_{D_OLP}	Power Limiting Debounce Time			43		ms
Z_{FB_IN}	FB Input Impedance			20		Kohm
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			250		ns
$V_{cs(max)}$	Current limiting threshold		0.97	1.0	1.03	V
T_{D_OCP}	Over Current Detection and Control Delay			70		ns
Oscillator Section						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
$\Delta F(shuffle)/F_{OSC}$	Frequency Shuffling Range		-4		4	%
D_{MAX}	Maximum Switching Duty Cycle			66.7		%
F_{Bust}	Burst Mode Base Frequency			22		KHz
On-chip Thermal Shutdown						
T_{SD}	Thermal Shutdown		---	165	--	°C
T_{RC}	Thermal Recovery			140	--	°C
GATE Driver Section (GATE pin)						
V_{OL}	Output Low Level	Igate_sink=20mA			1	V
V_{OH}	Output High Level	Igate_source=20mA	7.5			V
V_{G_clamp}	Output Clamp Level	VDD=24V		16		V
T_r	Output Rising Time	GATE=1nF		150		ns
T_f	Output Falling Time	GATE=1nF		60		ns

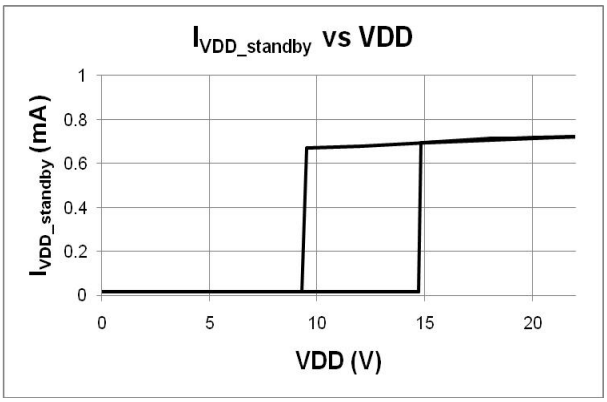
CHARACTERIZATION PLOTS

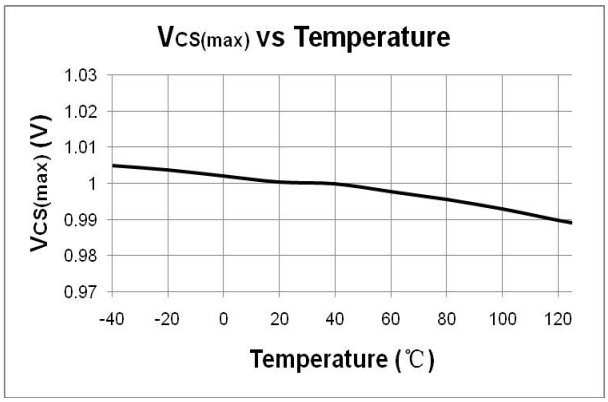












OPERATION DESCRIPTION

DP2269 is a highly integrated current mode PWM control IC optimized for high performance, low standby and cost effective offline flyback converter applications. The IC can achieve less than 75mW standby power and helps the design easily to meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of DP2269 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.

- **Operating Current**

The operating current of DP2269 is as low as 1.2mA. Good efficiency is achieved by the low operating current together with extended burst mode control schemes at No/light load conditions.

- **Soft Start**

DP2269 features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches UVLO(OFF), the peak current is gradually increased from nearly zero to the maximum level of 1V. Every restart up is followed by a soft start.

- **Oscillator with Frequency Shuffling**

PWM switching frequency in DP2269 is fixed to 65KHz and is trimmed to tight range. To improve system EMI performance, DP2269 operates the system with 4% frequency shuffling around setting frequency.

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in DP2269. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit is built in. During this blanking period (250ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

- **Synchronous Slope Compensation**

In DP2269, the synchronous slope compensation circuit is integrated by adding voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Extended Burst Mode Operation**

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.
DP2269 self adjusts the switching mode according to the loading condition. At no load or light load condition, the FB input is below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extension. The nature of high frequency switching also reduces the audio noise at any loading conditions.

- **Audio Noise Free Operation**

DP2269 can provide audio noise free operation from full loading to zero loading.

- **On-chip Thermal Shutdown (OTP)**

When the IC temperature is over 165 ^{O}C, the IC shuts down. Only when the IC temperature drops to 135 ^{O}C, IC will restart.

- **VDD OVP and Zener Clamp**

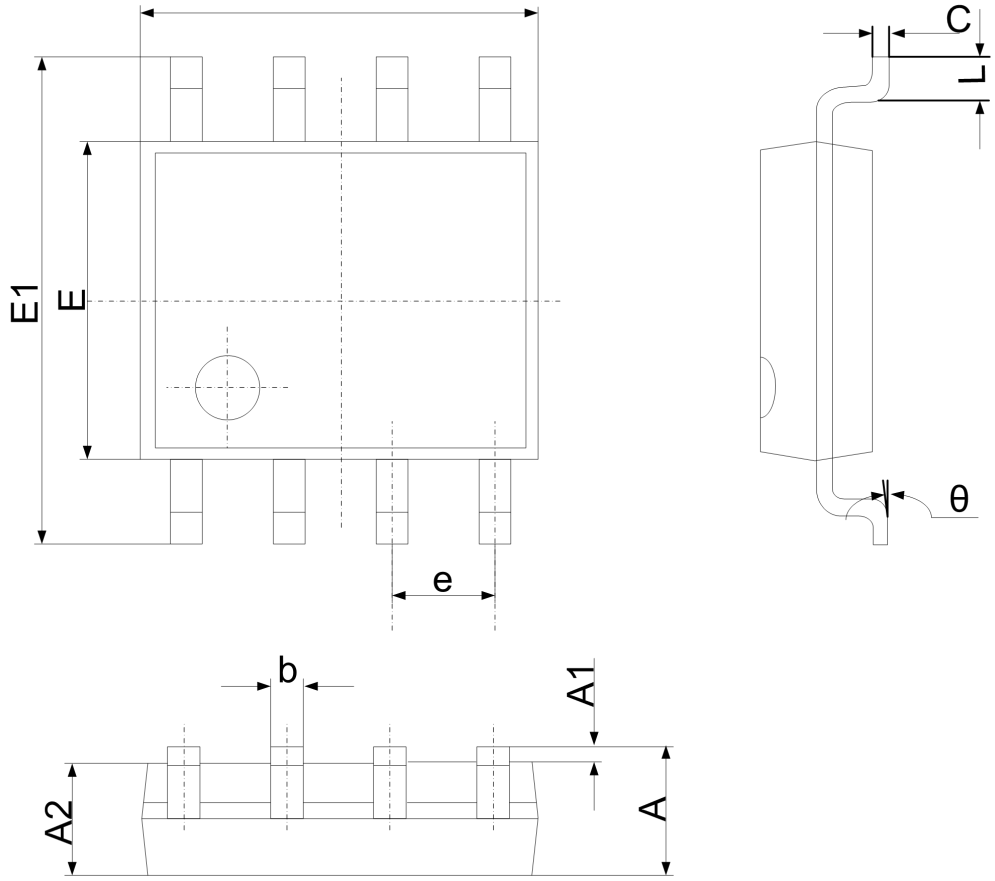
When VDD voltage is higher than 28.5V (typical), the IC will stop switching. This will cause VDD fall down to be lower than VDD_OFF (typical 9.4V) and then the system will restart up again. An internal 32V (typical) zener clamp is integrated to prevent the IC from damage.

- **Soft Gate Drive**

DP2269 has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.
Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Package Dimension

SOP8



符号	尺寸(毫米)		尺寸(英寸)	
	最小	最大	最小	最大
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (中心到中心)		0.050 (中心到中心)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°