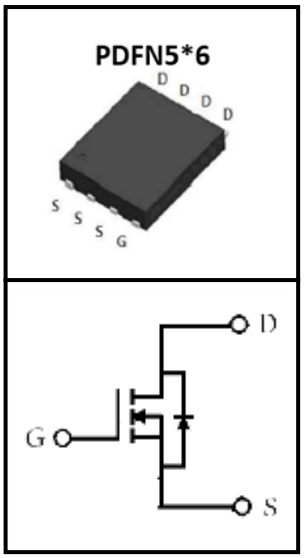
100V N-Channel Split Gate MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology



APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

RoHS

Device Marking and Package Information

Device	Package	Marking
CSN10N9P5B	PDFN5*6	CSN10N9P5B

Absolute Maximum Ratings at T_j= 25ºC unless otherwise noted

Parameter		Symbol	Value	Unit
Drain-Source Voltage (V_{GS} = 0V)		V_{DSS}	100	V
Continuous Drain Current T_C = 25ºC	(note1)	I_D	60	A
Continuous Drain Current T_C = 100ºC	(note1)		38	A
Pulsed Drain Current	(note2)	I_{DM}	240	A
Gate Source Voltage		V_{GSS}	±20	V
Single Pulse Avalanche Energy	(note3)	E_{AS}	14	mJ
Power Dissipation T_C = 25ºC	(note4)	P_D	63	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55~+150	ºC

Thermal Characteristics

Parameter		Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	(note1)	$R_{\theta JC}$	2.0	ºC/W
Thermal Resistance, Junction-to-Ambient	(note1)	$R_{\theta JA}$	55	ºC/W

Electrical Characteristics T_j= 25ºC unless otherwise specified						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V, T_J = 25ºC	--	--	1	uA
		V_{DS} = 100V, V_{GS} = 0V, T_J = 55ºC	--	--	5	uA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.2	2	2.6	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 20A	--	8.2	9.5	mΩ
		V_{GS} = 4.5V, I_D = 10A	--	11.3	14	mΩ
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1.0MHz	--	2122	--	pF
Output Capacitance	C_{oss}		--	618	--	
Reverse Transfer Capacitance	C_{rss}		--	25	--	
Gate Resistance	R_g	V_{GS} = 0V,f = 1.0MHz	--	1.94	--	Ω
Total Gate Charge	Q_g	V_{DD} = 50V, I_D = 20A, V_{GS} = 10V	--	41.8	--	nC
Gate-Source Charge	Q_{gs}		--	9	--	
Gate-Drain Charge	Q_{gd}		--	10	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 50V, I_D = 20A V_{GS} = 10V,R_G = 3Ω	--	17	--	ns
Turn-on Rise Time	t_r		--	4	--	
Turn-off Delay Time	$t_{d(off)}$		--	32	--	
Turn-off Fall Time	t_f		--	8	--	
Body Diode Characteristics						
Source-Drain Current(Body Diode)	I_{SD}		--	--	60	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 20A, V_{GS} = 0V	--	0.88	1.0	V
Reverse Recovery Time	t_{rr}	T_J = 25ºC, I_F = 20A di_F/dt = 100A/μs	--	50.5	--	ns
Reverse Recovery Charge	Q_{rr}		--	71.5	--	nC

Notes

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width≦300us , duty cycle≦2%
3. The EAS data shows Max. rating . The test condition is VDD =50V,VGS =10V,L=0.5mH
4. The power dissipation is limited by 175℃ junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics T_J = 25ºC, unless otherwise noted

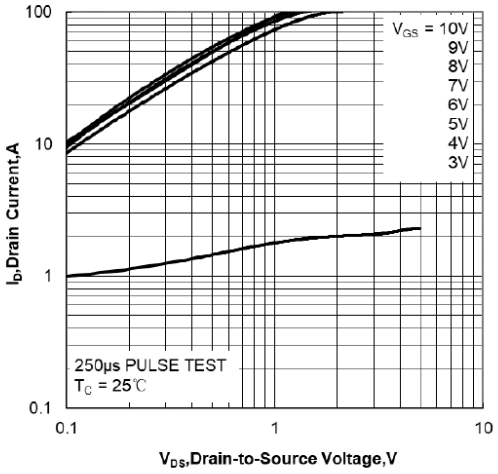


Figure 1. Output Characteristics

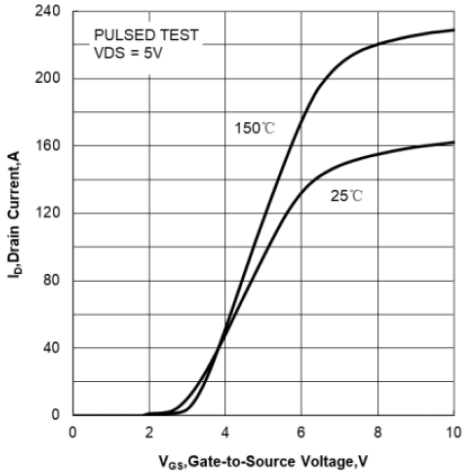


Figure 2. Transfer Characteristics

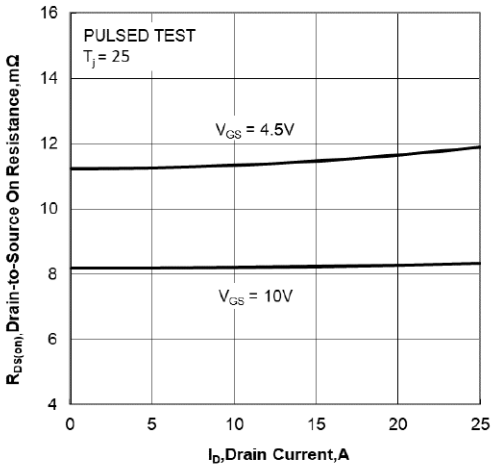


Figure 3. Drain-to-Source On Resistance vs Drain Current

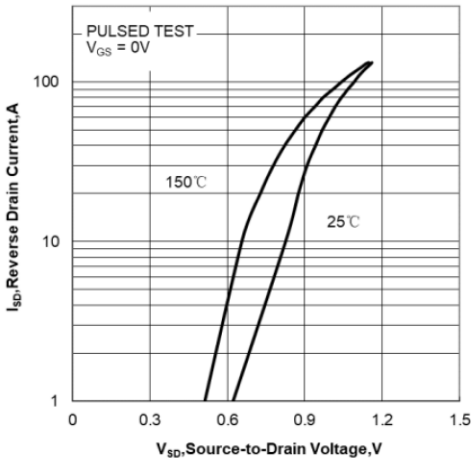


Figure 4. Body Diode Forward Voltage vs Source Current and Temperature

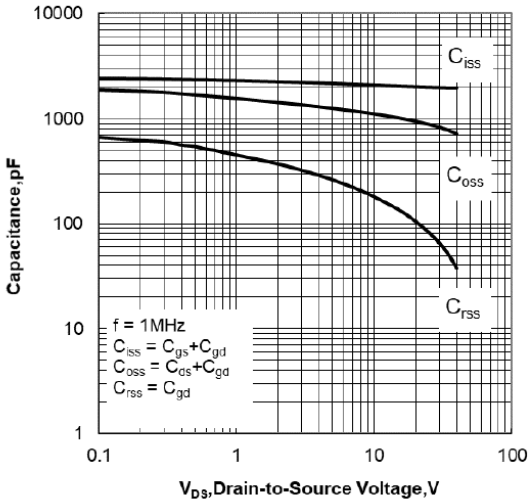


Figure 5. Capacitance Characteristics

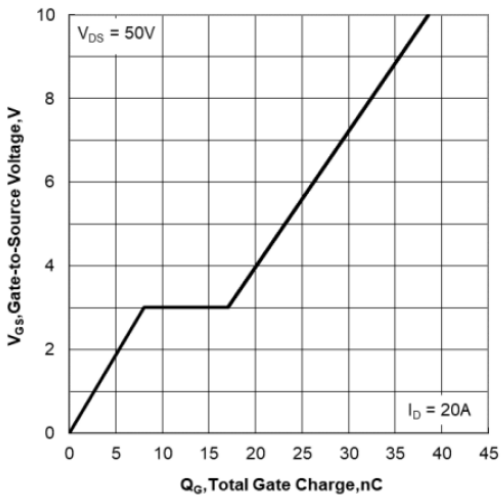


Figure 6. Gate Charge Characteristics

Typical Characteristics T_J = 25ºC, unless otherwise noted

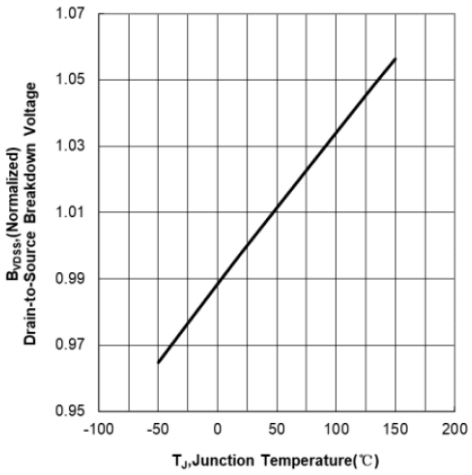


Figure 7. Normalized Breakdown Voltage vs Junction Temperature

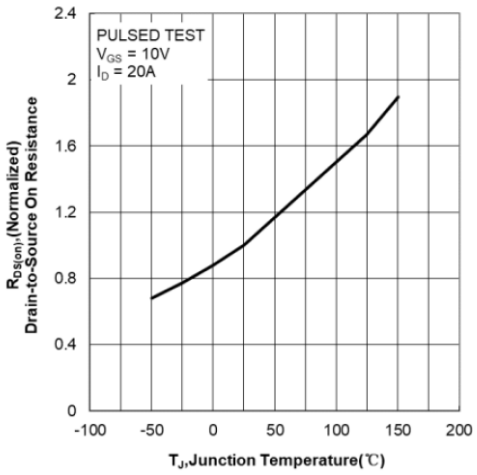


Figure 8. Normalized On Resistance vs Junction Temperature

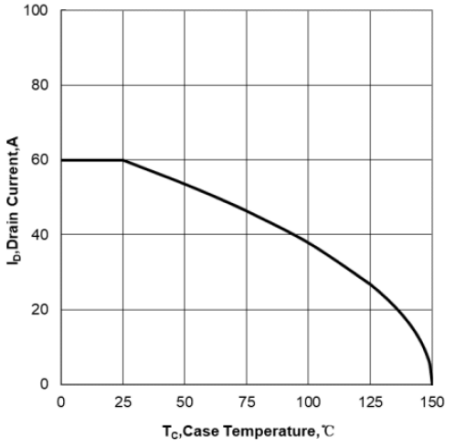


Figure 9. Maximum Continuous Drain Current vs Case Temperature

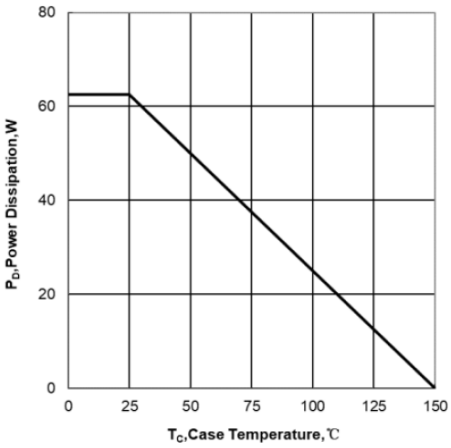


Figure 10. Maximum Power Dissipation vs Case Temperature

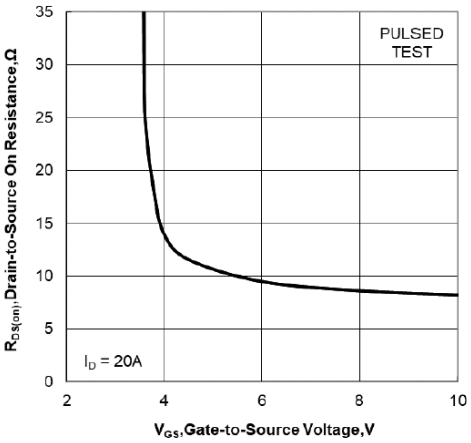


Figure11. Drain-to-Source On Resistance vs Gate Voltage and Drain Current

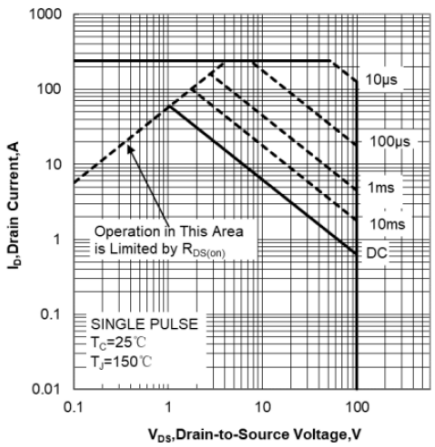


Figure 12. Maximum Safe Operating Area

Typical Characteristics T_J = 25ºC, unless otherwise noted

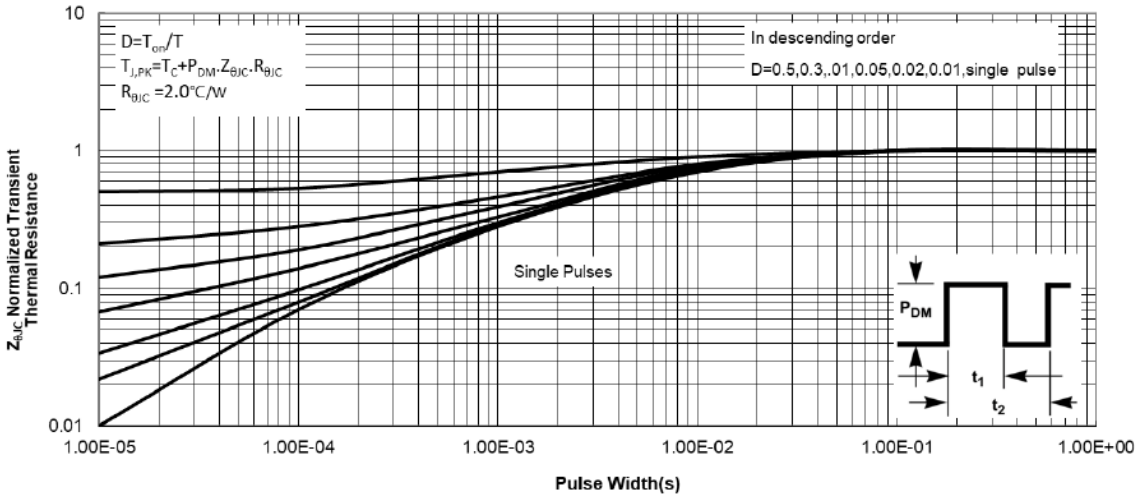


Figure 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Figure A：Gate Charge Test Circuit and Waveform

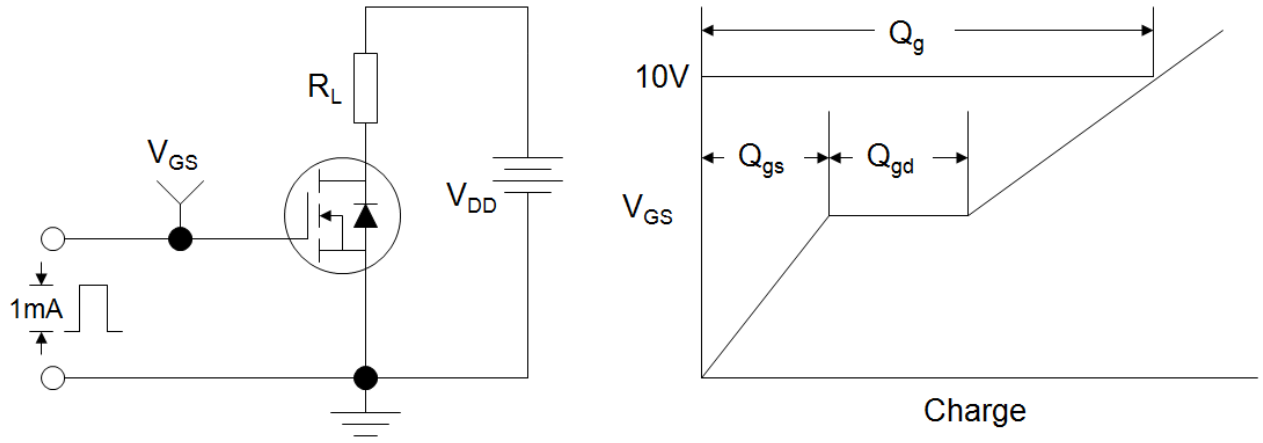


Figure B：Resistive Switching Test Circuit and Waveform

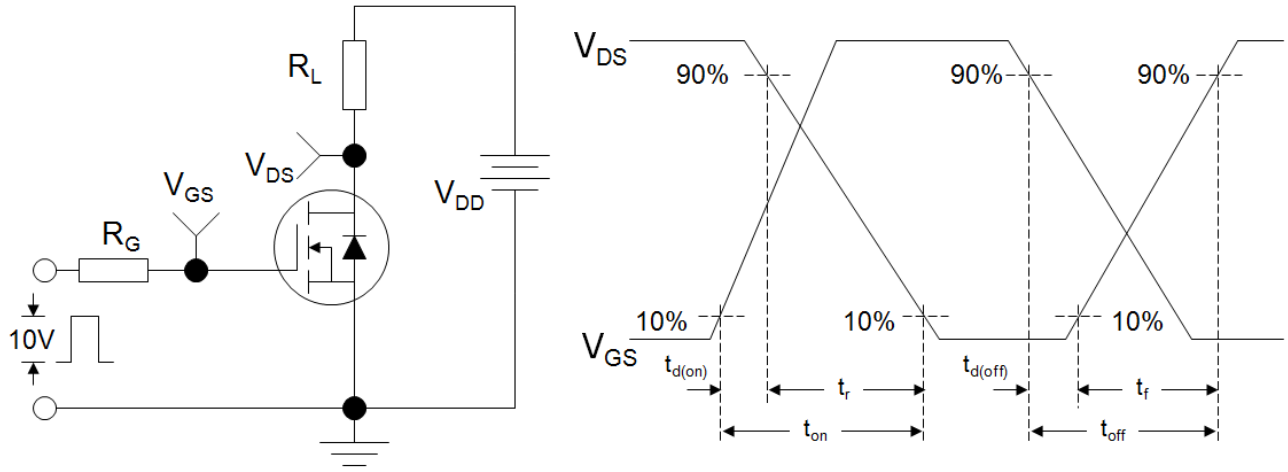
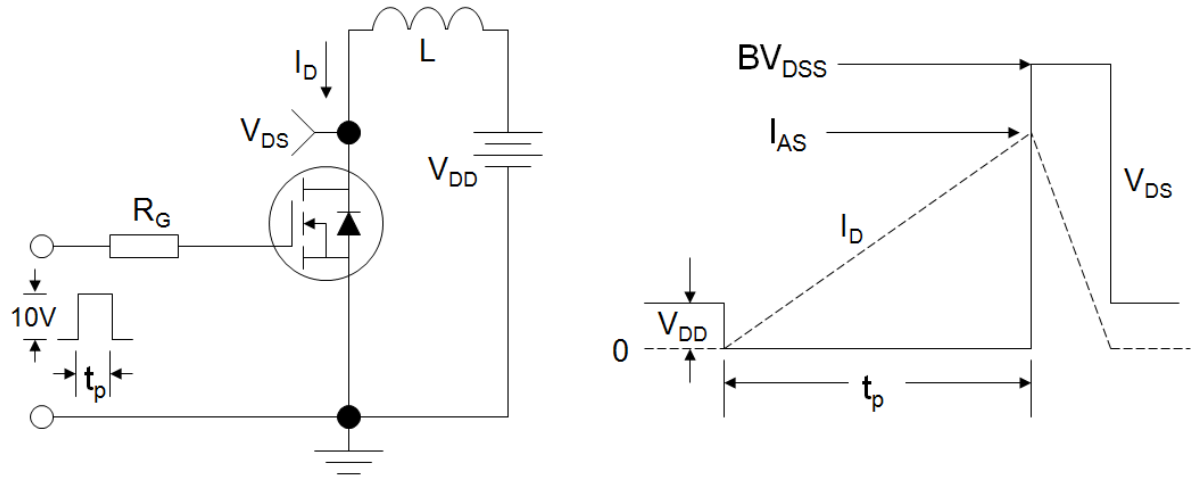


Figure C：Unclamped Inductive Switching Test Circuit and Waveform



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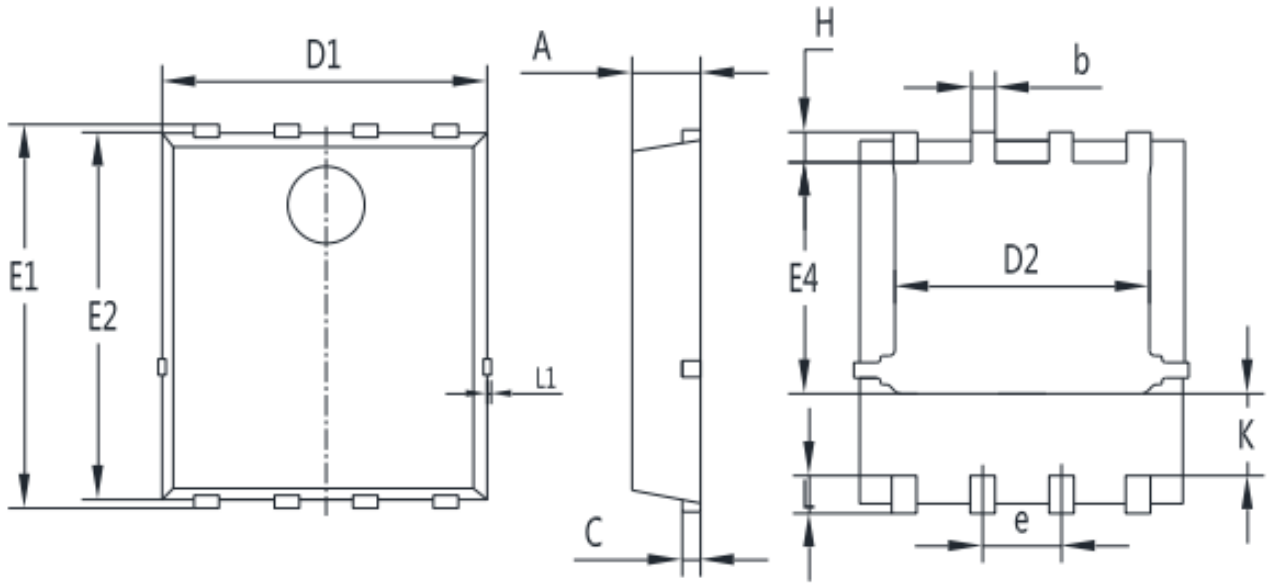

SYMBOLS	MILLIMETERS	
	MIN	MAX
A	1.00	1.20
b	0.30	0.50
c	0.15	0.35
D1	5.00	5.40
D2	3.80	4.25
e	1.17	1.37
E1	5.95	6.35
E2	5.66	6.06
E4	3.52	3.92
H	0.40	0.60
L	0.30	0.70
L1	0.12REF	
K	1.15	1.45

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