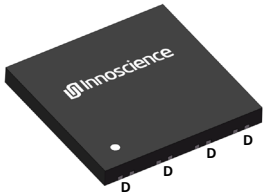
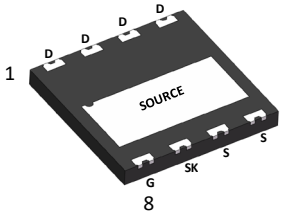
INN650DA04

650V GaN Enhancement-mode Power Transistor

Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard





Gate	8
Drain	1,2,3,4
Kelvin Source	7
Source	5,6

Benefits

- High efficiency power switching
- High power density
- Enables higher switching frequency
- System cost savings

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

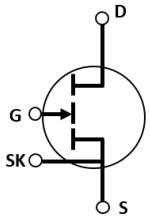


Table 1 Key Performance Parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$	400	mΩ
$Q_{G,typ}$	0.9	nC
$I_{DS,Pulse}$	11	A
Q_{OSS} @ 400V	9	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Type/Ordering Code	Package	Marking
INN650DA04	DFN 5X6	INN650DA04

Table of contents

1 Maximum ratings

at T_j = 25 °C unless otherwise specified.
Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain source voltage	$V_{DS,max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 μA
Drain source voltage transient [1]	$V_{DS(transient)}$	-	-	750	V	V_{GS} = 0 V, V_{DS} = 750 V
Continuous current, drain source	I_D	-	-	7	A	T_c = 25 °C
Pulsed current, drain source [2]	$I_{D,pulse}$	-	-	11	A	T_c = 25 °C; V_G = 6 V; See Figure 16;
Pulsed current, drain source [2]	$I_{D,Pulse}$	-	-	6	A	T_c = 125 °C;V_G = 6 V; See Figure 17;
Gate source voltage, continuous [3]	V_{GS}	-1.4	-	+7	V	Tj = -55 °C to 150 °C
Gate source voltage, pulsed	$V_{GS,pulse}$	-20	-	+10	V	Tj = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz open drain
Power dissipation	P_{tot}	-	-	39	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	˚C	
Storage temperature	T_{stg}	-55	-	+150	˚C	

1 $V_{DS(transient)}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs

2 Pulse = 300 μs

3 The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance，junction-case	R_{thJC}	-	-	3.2	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.6	2.2	V	I_D = 5.2 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.7	-		I_D = 5.2 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	0.4	10	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	5	80		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	4	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	368	400	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 25 °C
		-	750	-	mΩ	V_{GS} = 6 V; I_D = 2 A; T_j = 150 °C
Gate resistance	R_G	-	3	-	Ω	F = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	34	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Output capacitance	C_{oss}	-	9	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Reverse transfer capacitance	C_{rss}	-	0.4	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	13	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	20	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output Charge	Q_{OSS}	-	9	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V

1 $C_{O(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

2 $C_{O(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	0.9	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D= 2 A
Gate-source charge	Q_{GS}	-	0.1	-	nC	
Gate-drain charge	Q_{GD}	-	0.3	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.7	-	V	V_{DS} = 400 V; I_D= 2 A

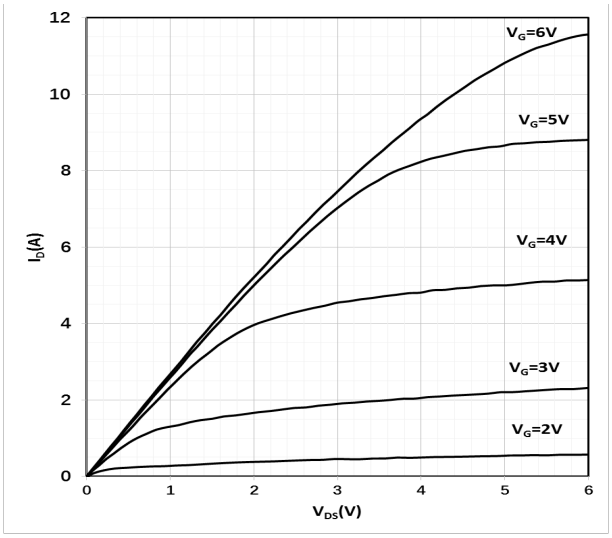
Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	3	-	V	V_{GS} = 0 V; I_{SD}= 2 A
Pulsed current, reverse	$I_{S,pulse}$	-	-	11	A	V_G = -4 V
Reverse recovery charge	Q_{rr}	-	0	-	nC	I_{SD} =2 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

4 Electrical characteristics diagrams

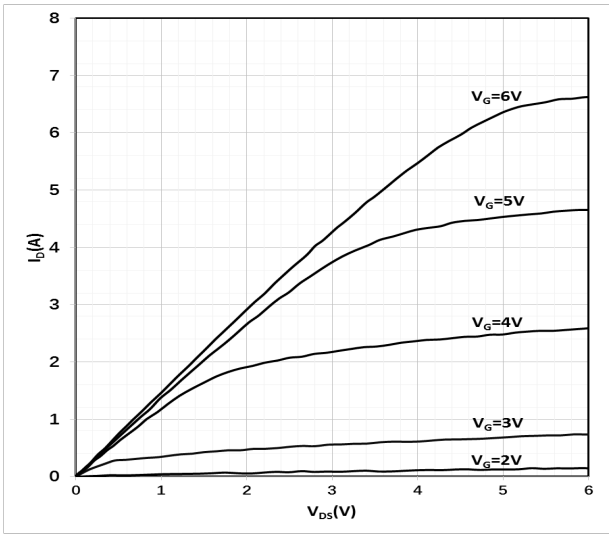
at T_j = 25 °C, unless specified otherwise

Figure 1 Typ. output characteristics



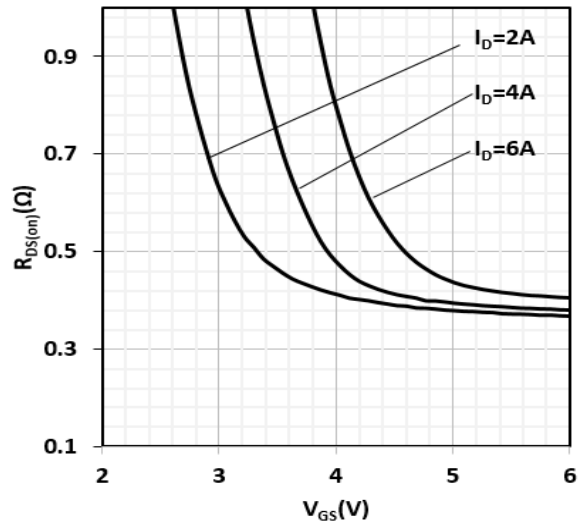
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



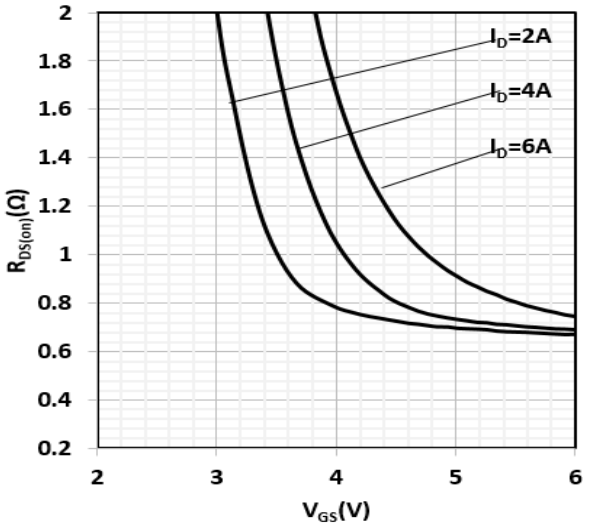
$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 3 Typ. Drain-source on-state resistance



$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 25 °C

Figure 4 Typ. Drain-source on-state resistance



$R_{DS(on)} = f(I_{DS},V_{GS})$; T_j = 125 °C

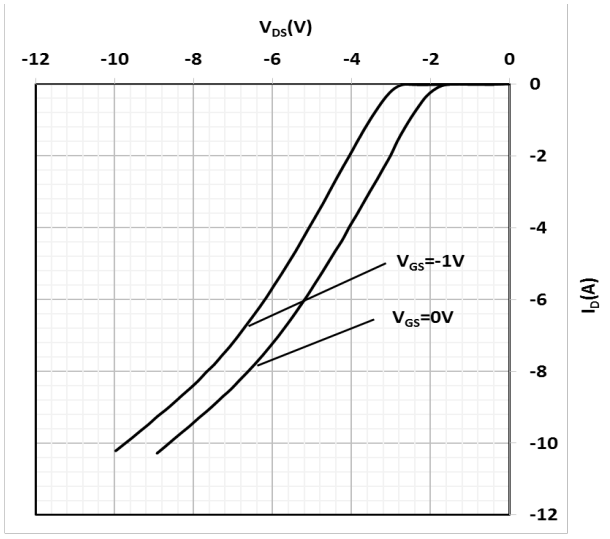
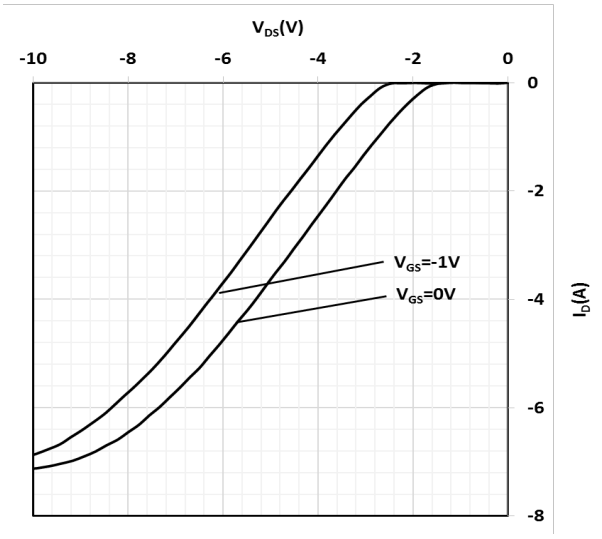
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS},V_{GS})$; T_j= 25 °C	$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

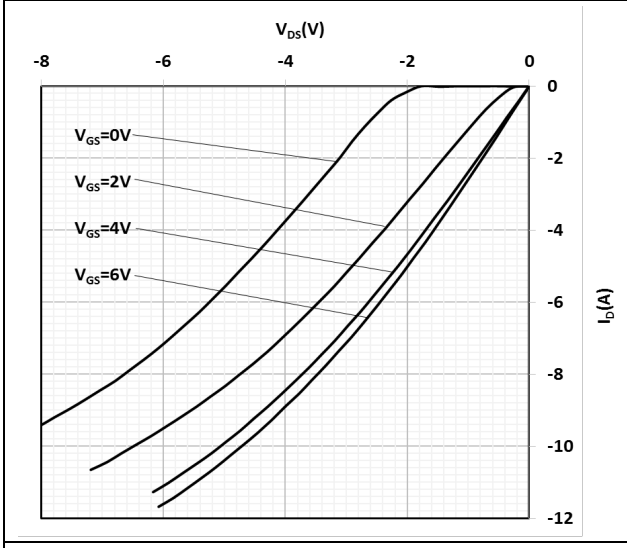
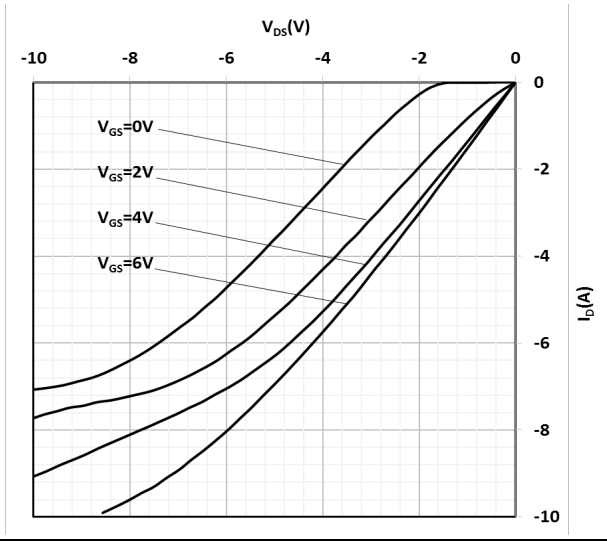
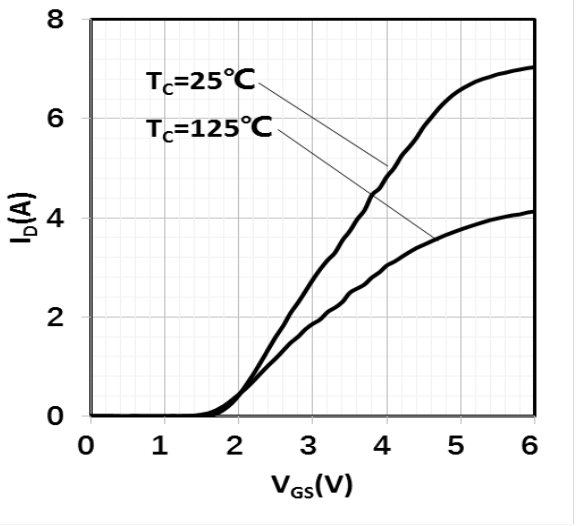
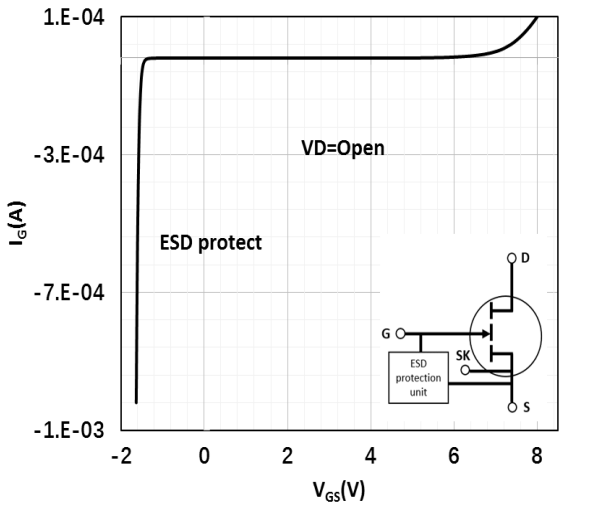
Figure 7 Typ. channel reverse characteristics	Figure 8 Typ. channel reverse characteristics
	
$I_D = f(V_{DS},V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS},V_{GS})$; T_j = 125 °C

Figure 9 Typ. transfer characteristics



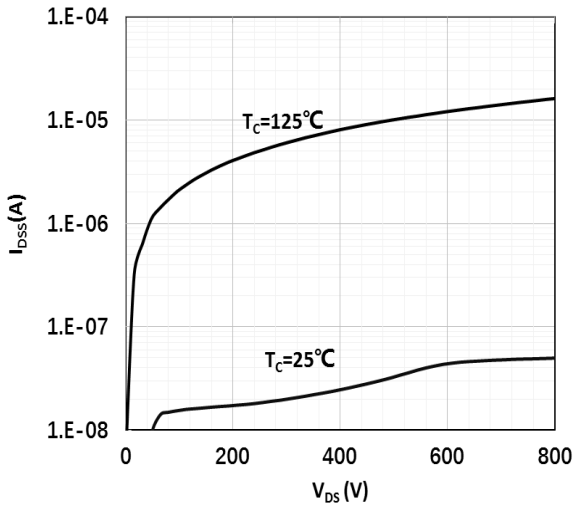
$I_D = f(V_{GS})$; V_{DS}= 3 V

Figure 10 Typ. Gate-to-Source leakage



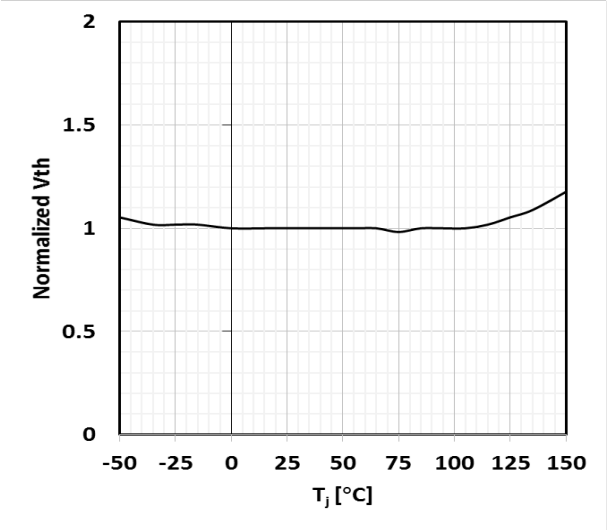
$I_G = f(V_{GS})$; Ig reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



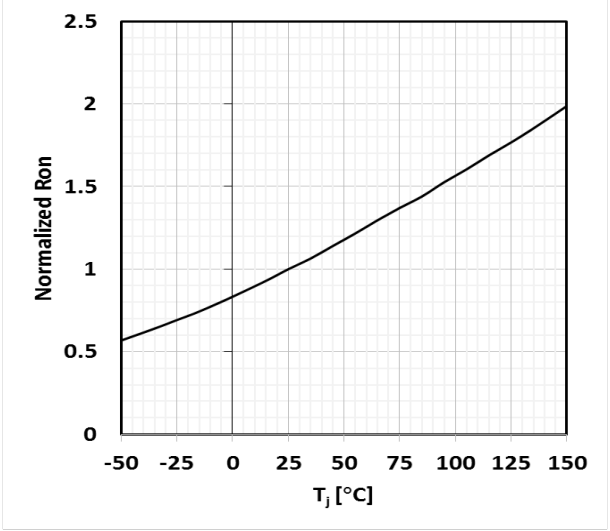
$I_{DSS} = f(V_{DS})$; V_{GS} = 0 V

Figure 12 Gate threshold voltage



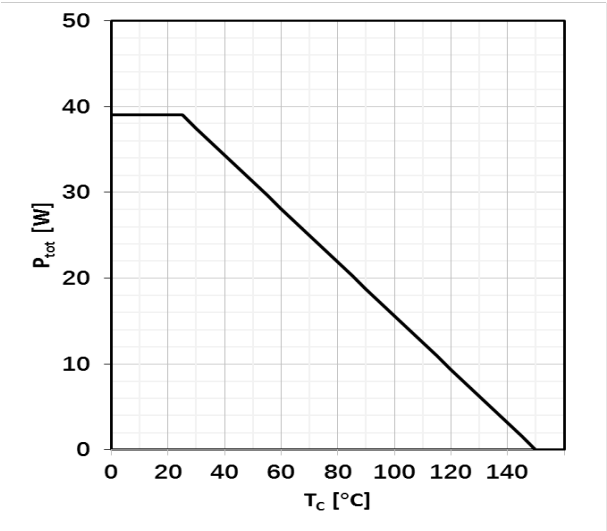
$V_{TH} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 5.2 mA

Figure 13 Drain-source on-state resistance



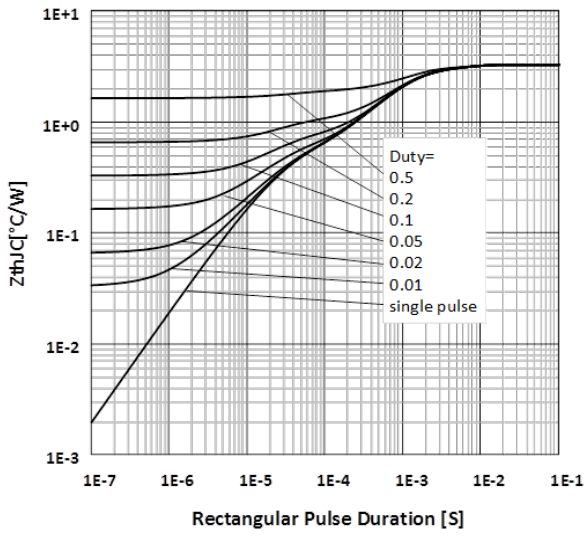
$R_{DS(on)} = f(T_j)$; I_D = 2 A; V_G=6V

Figure 14 Power dissipation



$P_{tot} = f(T_C)$

Figure 15 Max.transient thermal impedance



$Z_{thJC} = f(t_P, D)$

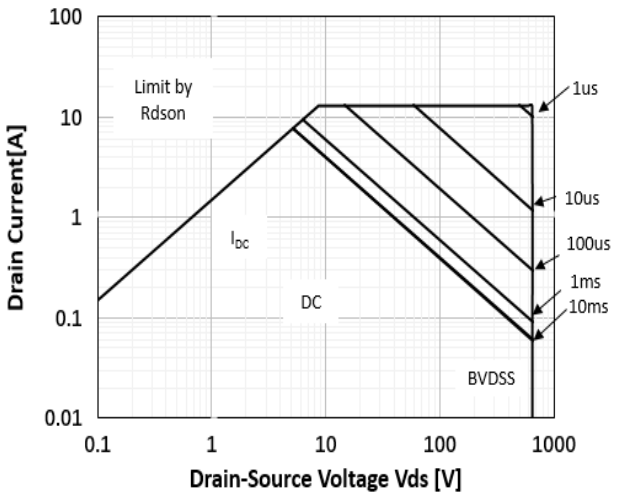
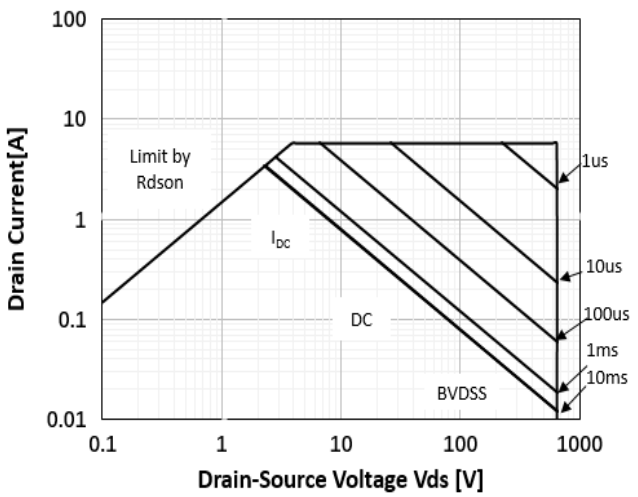
Figure 16 Safe operating area	Figure 17 Safe operating area
	
$I_D = f(V_{DS})$; $T_C = 25$ °C	$I_D = f(V_{DS})$; $T_C = 125$ °C

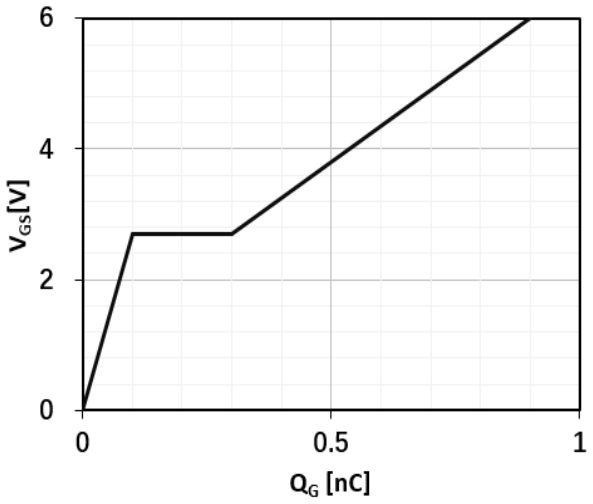
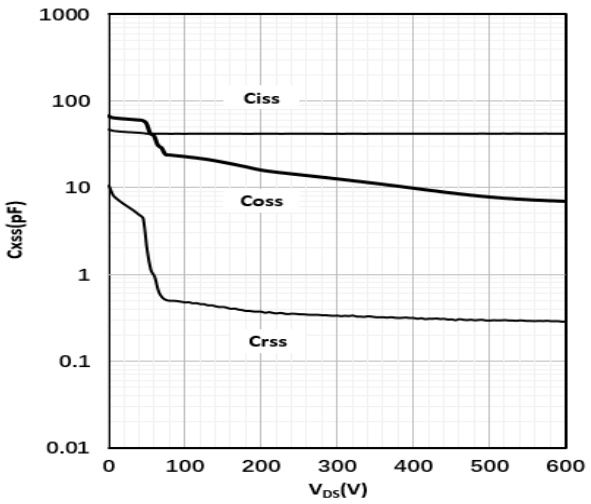
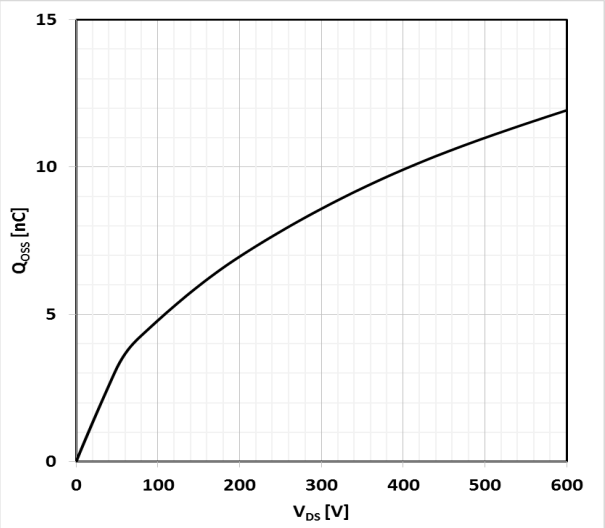
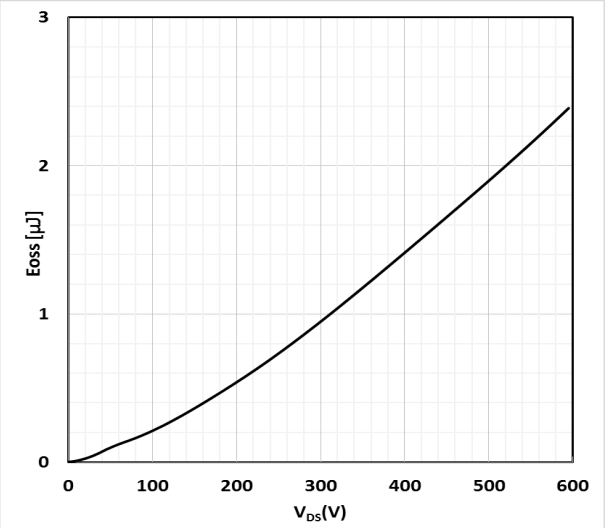
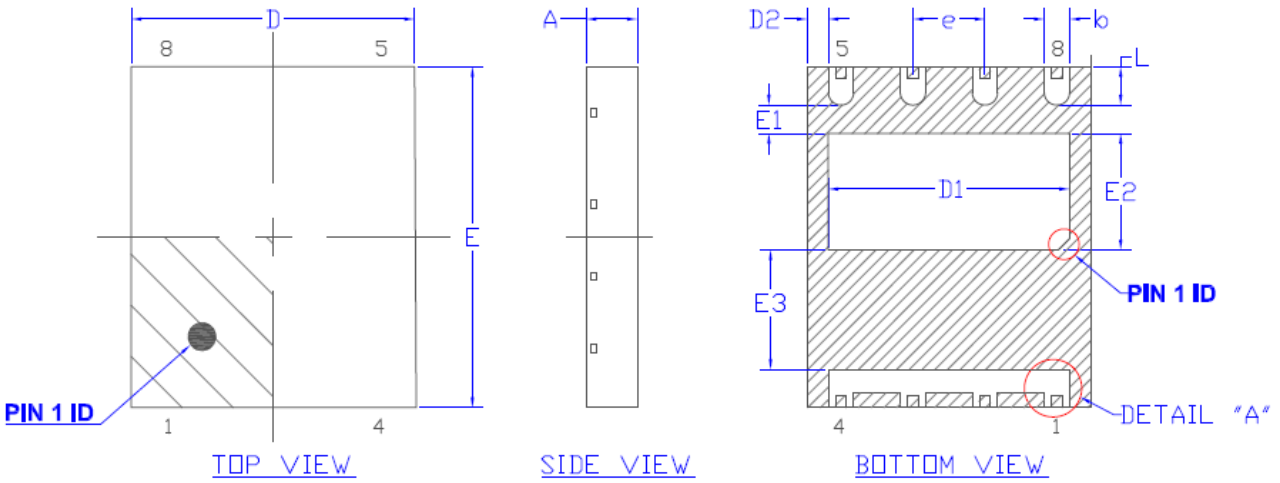
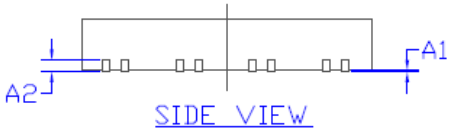
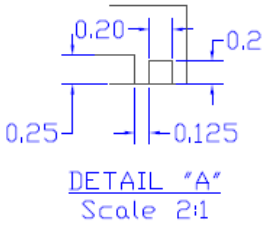
Figure 18 Typ. gate charge	Figure 19 Typ. capacitances
	
$V_{GS} = f(Q_G)$; $V_{DCLINK} = 400$ V; $I_D = 2$ A	$C_{XSS} = f(V_{DS})$； Freq. = 100 kHz

Figure 20 Typ. output charge	Figure 21 Typ. C_{OSS} stored Energy
	
$Q_{OSS} = f(V_{DS})$；Freq. = 100 kHz	$E_{OSS} = f(V_{DS})$；Freq. = 100 kHz

5 Package outlines







SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	---	0.203 Ref	---
b	0.40	0.45	0.50
D		5.00 B.S.C	
D1	4.16	4.26	4.36
D2	0.27	0.37	0.47
E		6.00 B.S.C	
E1	0.40	0.50	0.60
E2	1.95	2.05	2.15
E3	---	2.10	---
e		1.27 B.S.C	
L	0.575	0.675	0.775

Notes:

(1) Dimension and tolerance conform to ASME Y14.5-2009.

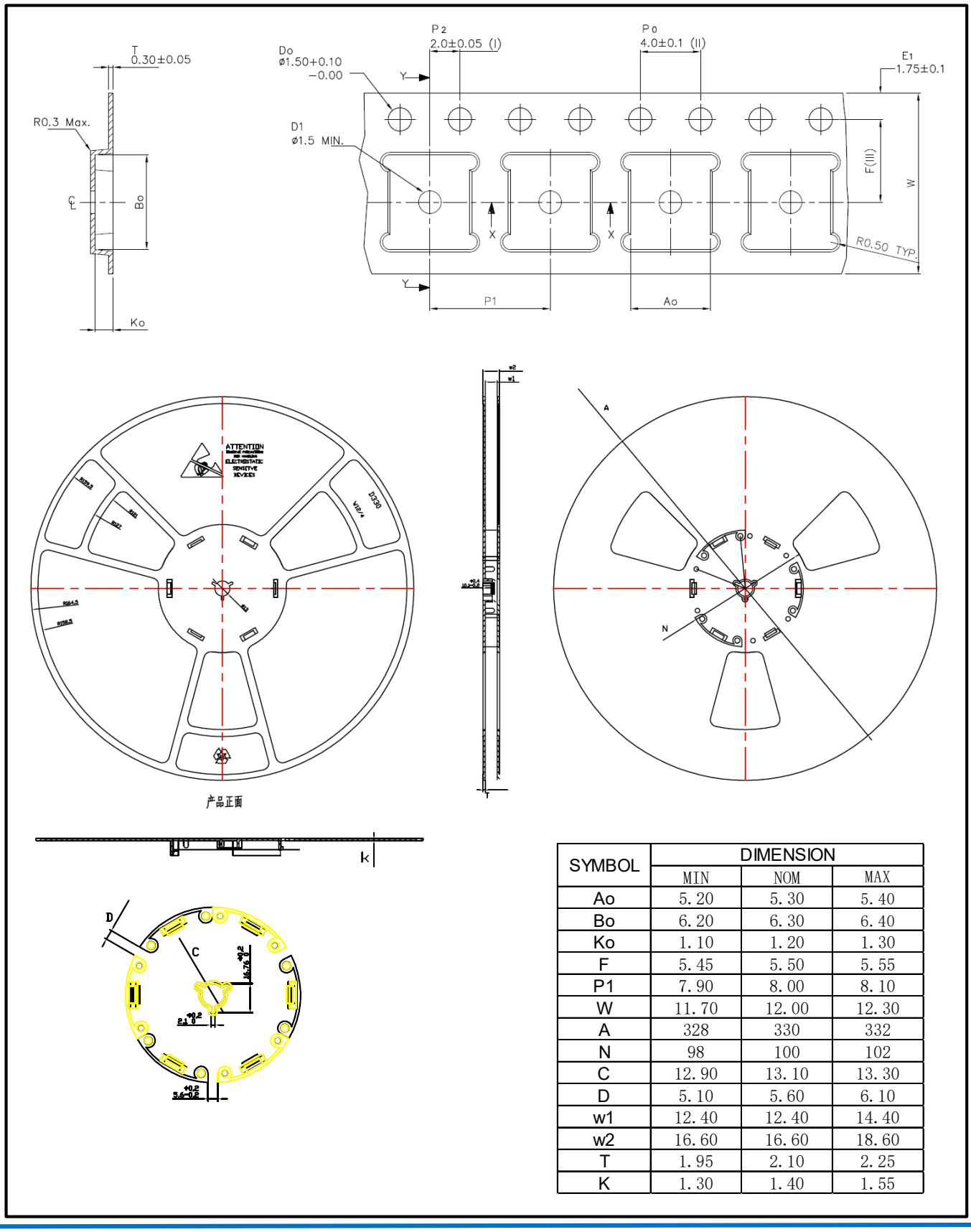
(2) All Dimensions are in millimeters.

(3) Lead coplanarity shall be 0.1 millimeters max.

(4) Complies with JEDEC MO-229.

(5) Drawing is not to scale.

6 Reel information



SYMBOL	DIMENSION		
	MIN	NOM	MAX
Ao	5.20	5.30	5.40
Bo	6.20	6.30	6.40
Ko	1.10	1.20	1.30
F	5.45	5.50	5.55
P1	7.90	8.00	8.10
W	11.70	12.00	12.30
A	328	330	332
N	98	100	102
C	12.90	13.10	13.30
D	5.10	5.60	6.10
w1	12.40	12.40	14.40
w2	16.60	16.60	18.60
T	1.95	2.10	2.25
K	1.30	1.40	1.55

7 Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2021-1-28	Preliminary version release