

MOSFET Silicon N-Channel MOS

1. Applications

Boost PFC switch, Half bridge or Asymmetric half bridge or Series resonance half bridge and full bridge topologies.
Server power, Telecom power, EV charging, Solar inverter, UPS Application.



2. Features

Low drain-source on-resistance: $R_{DS(ON)} = 0.095\Omega$ (typ.)
Easy to control Gate switching
Enhancement mode: $V_{th} = 2.8$ to 4.2 V

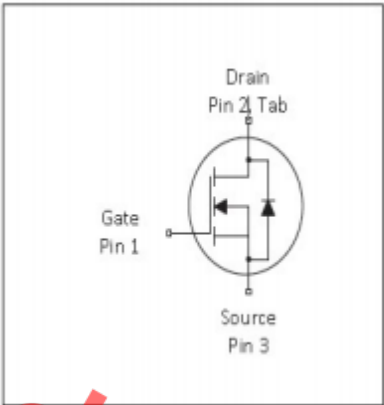
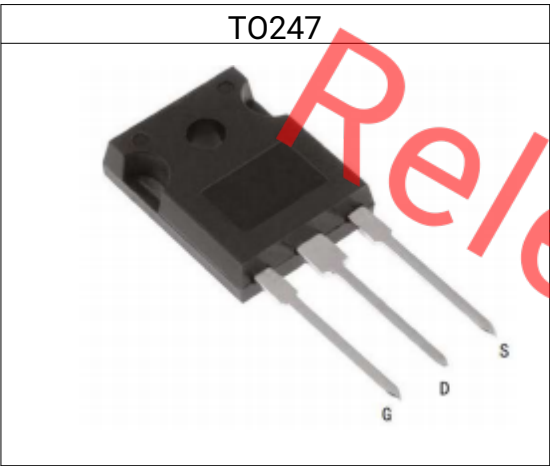


Table 1 Key PerformanceParameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	110	mΩ
$Q_{g,typ}$	52	nC
$I_{D,pulse}$	120	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
ASW65R110E	T0247	ASW65R110E



1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D		-	40	A	$T_C = 25^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	120	A	$T_C = 25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	2528	mJ	
MOSFET dv/dt ruggedness	dv/dt	-	-	36	V/ns	$V_{DS} = 0 \dots 400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	277.8	W	$T_C = 25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS} = 0 \dots 400\text{V}$, $I_{SD} \leq 48\text{A}$, $T_j = 25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_{θ}

Released

2 Thermalcharacteristics

Table 3 Thermalcharacteristics

Parameter				Symbol	Values			Unit	Note / Test Condition
					Min.	Typ.	Max.		
Thermal resistance, junction - case				R_{thJC}	-	-	0.45	°C/W	-
Thermal resistance, junction - ambient				R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

Released

3 Electrical characteristics

at $T_j=25^{\circ}\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	655	-	-	V	$V_{GS}=0V, I_D=10mA$
Gate threshold voltage	$V_{(GS)th}$	2.8		4.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650V, V_{GS}=0V, T_j=25^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.095	0.110	Ω	$V_{GS}=10V, I_D=14A, T_j=25^{\circ}\text{C}$
Gate resistance (Intrinsic)	R_G	-	13.4	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2497	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Output capacitance	C_{oss}	-	239	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Reverse transfer capacitance	C_{rss}	-	6.75	-	pF	$V_{GS}=0V, V_{DS}=50V, f=10kHz$
Turn-on delay time	$t_{(on)}$	-	23	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2\Omega$; see table 9
Rise time	t_r	-	28	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2\Omega$; see table 9
Turn-off delay time	$t_{(off)}$	-	108.4	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2\Omega$; see table 9
Fall time	t_f	-	24	-	ns	$V_{DD}=400V, V_{GS}=10V, I_D=25A, R_G=2\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition		
		Min.	Typ.	Max.				
Gate to source charge	Q_{gs}	-	7.1	-	nC	$V_{DD}=400V, I_D=25A, V_{GS}=0$	to	10V
Gate to drain charge	Q_{gd}	-	20	-	nC	$V_{DD}=400V, I_D=25A, V_{GS}=0$	to	10V
Gate charge total	Q_g	-	52	-	nC	$V_{DD}=400V, I_D=25A, V_{GS}=0$	to	10V
Gate plateau voltage	$V_{plateau}$	-	9	-	V	$V_{DD}=400V, I_D=25A, V_{GS}=0$	to	10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.69	-	V	$V_{GS}=0V, I_F=1A, T_J=25^{\circ}C$
Reverse recovery time	t_r	-	380.8	-	ns	$V_R=400V, I_F=25A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	8.8	-	uC	$V_R=400V, I_F=25A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	45.2	-	A	$V_R=400V, I_F=25A, di_F/dt=100A/\mu s$; see table 8

Released

4 Electrical characteristics diagram

Diagram 1: Typ. output characteristics

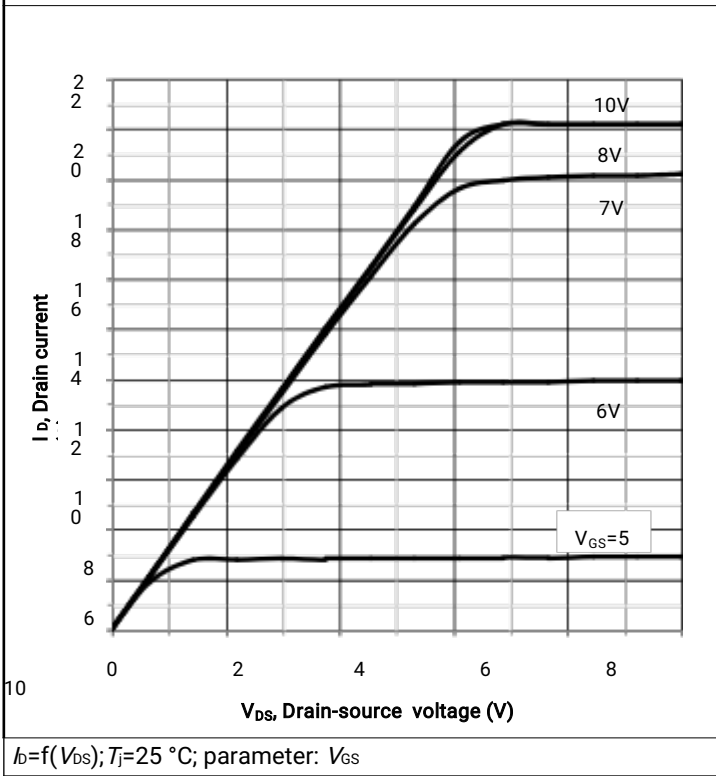


Diagram 2: Typ. Coss stored energy

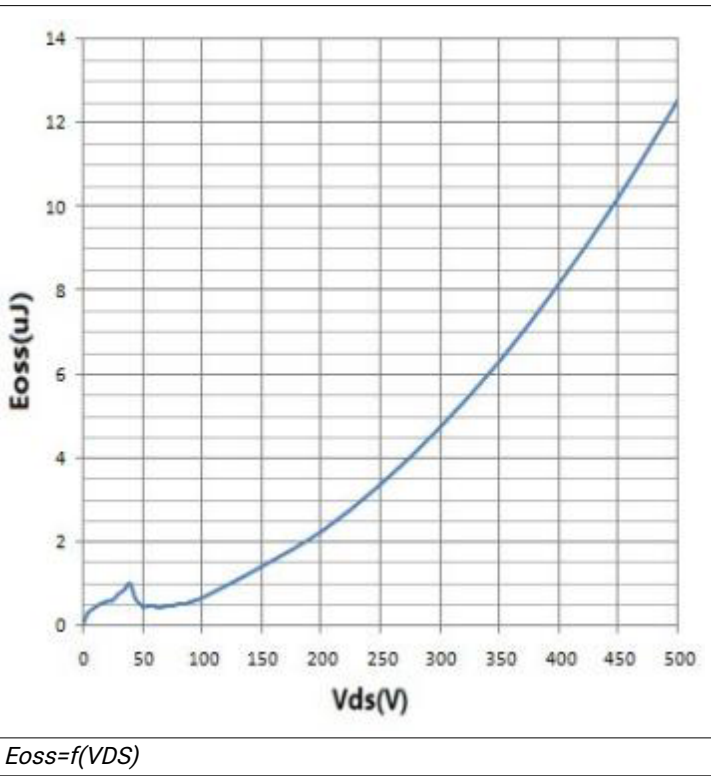


Diagram 3: Typ. transfer characteristics

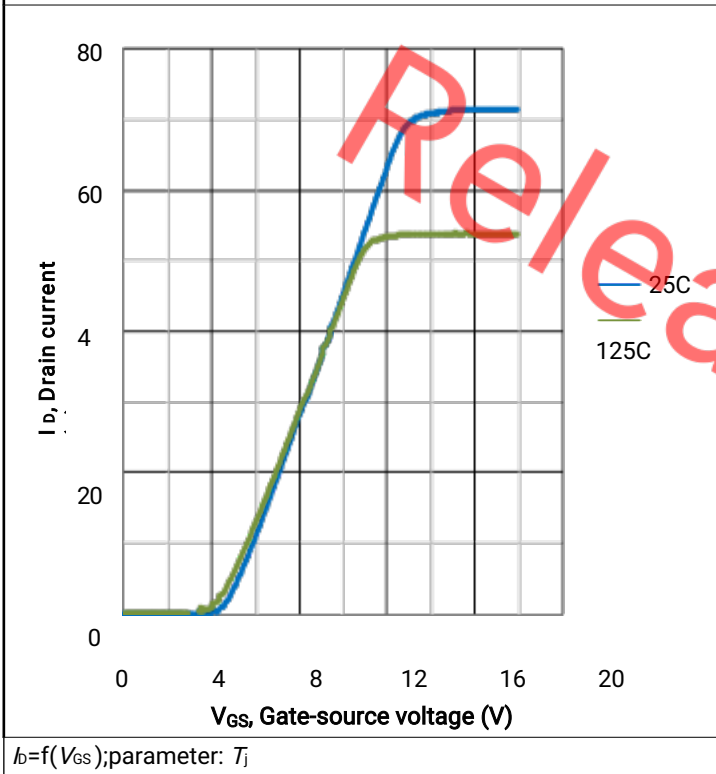


Diagram 4: Typ. gate charge

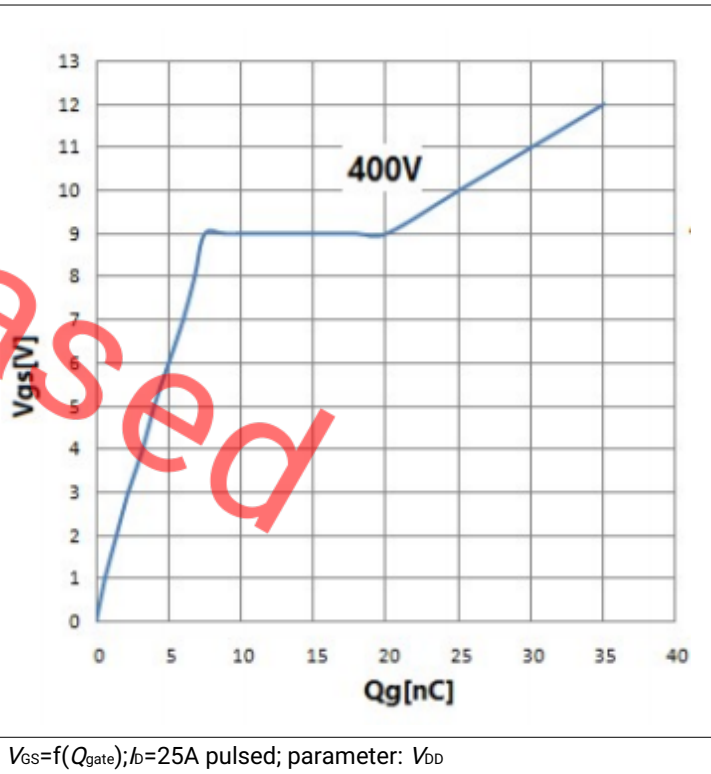
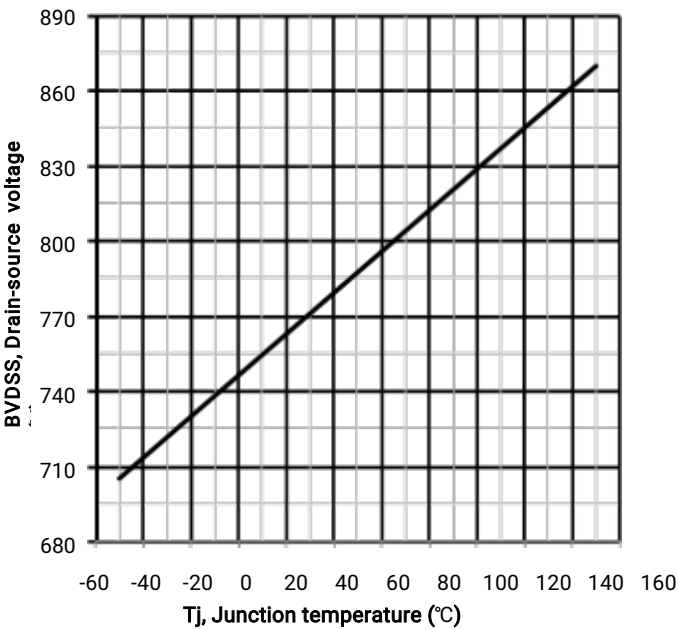
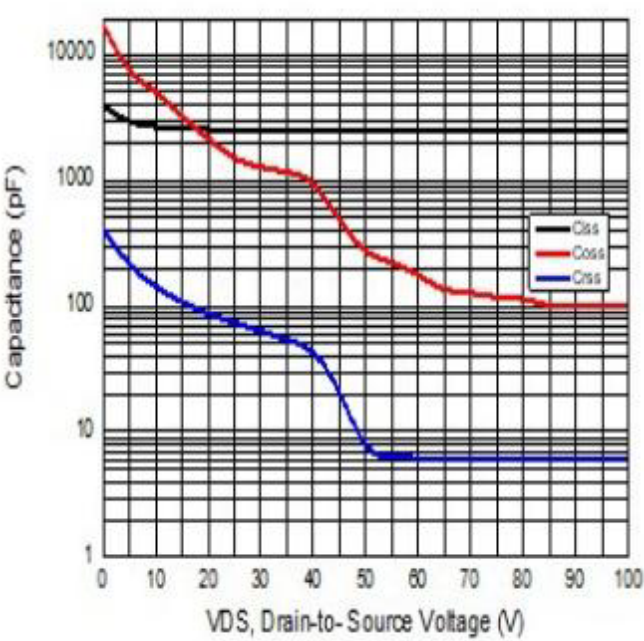


Diagram 5: Drain-source breakdown voltage



$V_{BR(DSS)} = f(T_j); I_D = 10\text{mA}$

Diagram 6: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0\text{V}; f = 10\text{ kHz}$

Released

5 TestCircuits

Table 8 Diodecharacteristics

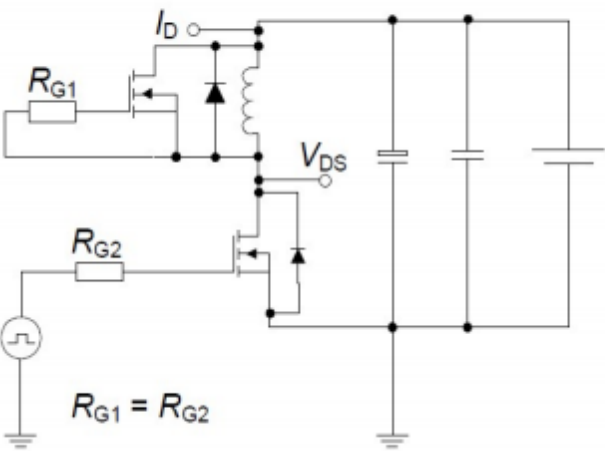
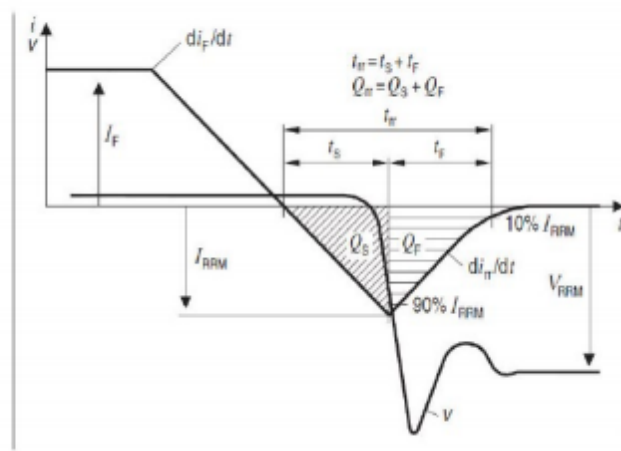
Test circuit for diode characteristics	Diode recovery waveform
 $R_{G1} = R_{G2}$	

Table 9 Switchingtimes

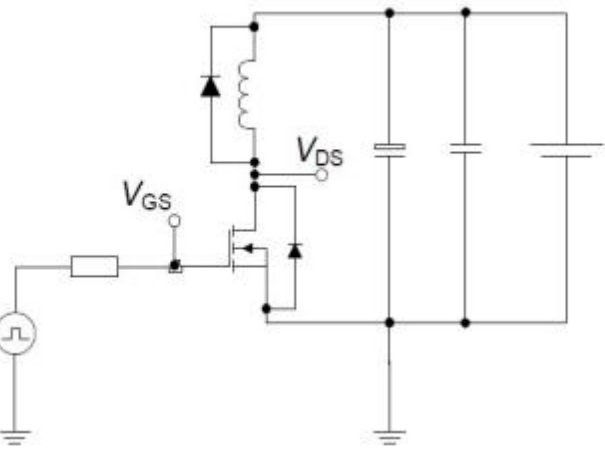
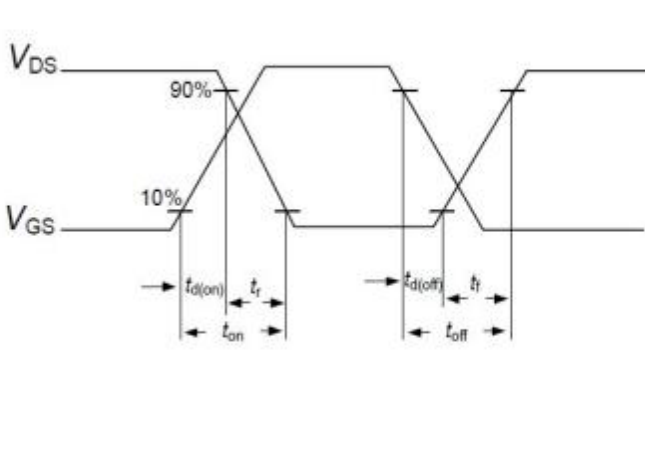
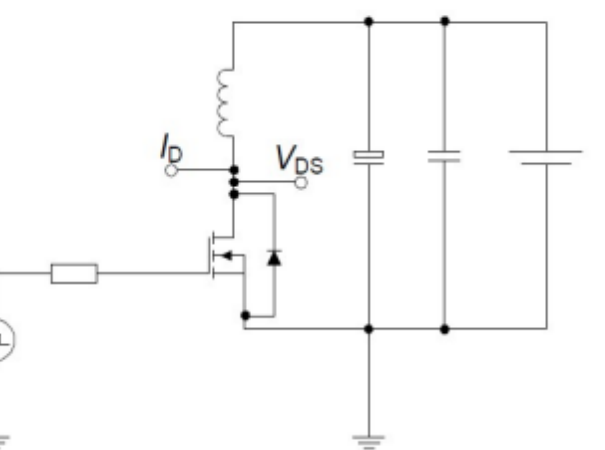
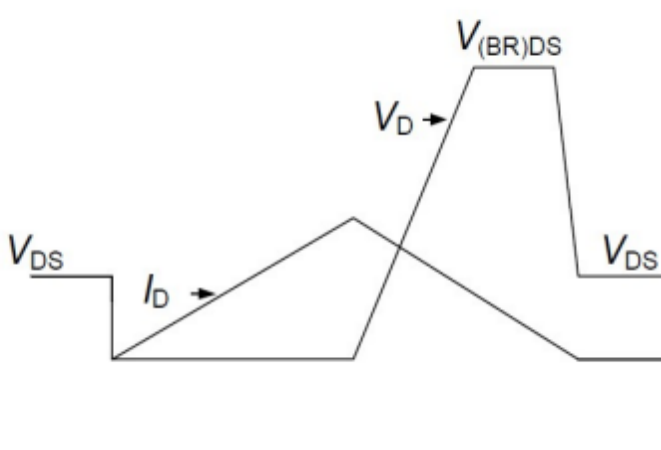
Switching times test circuit for inductive load	Switching times waveform
	

Table10 Unclamped inductiveload

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 PackageOutlines

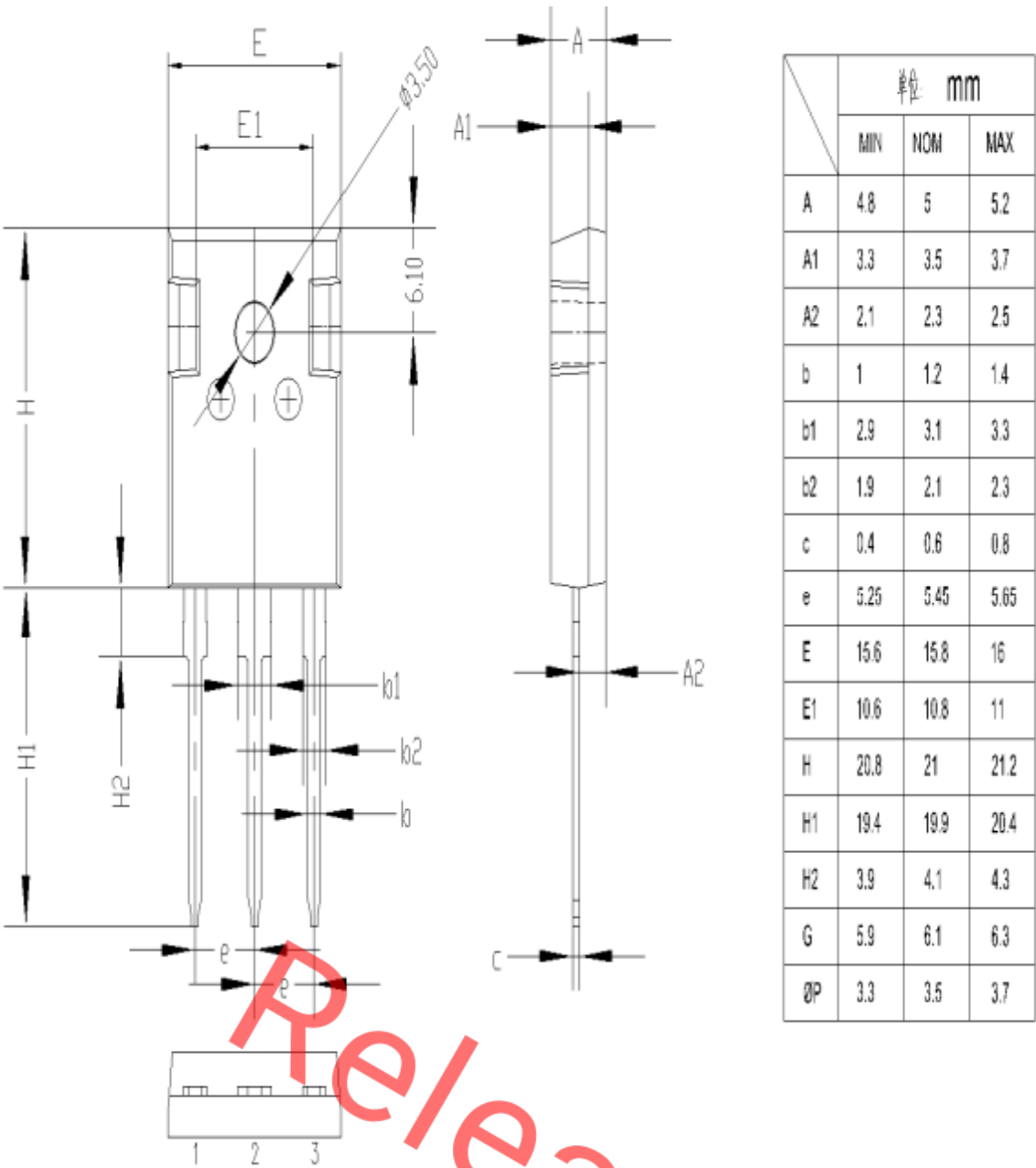


Figure1 : Outline PG-T0247

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2020-03-05	Release version
2.0	2020-03-19	Add Electrical characteristics Curve

Released