CHIPLINK N-Channel Enhancement Mode Power MOSFET

Description

The LX3030N combines advanced trench technology to provide excellent $R_{DS(ON)}$, it tailored to minimize conduction loss, and provide superior switching performance. It can be used in wide variety of application.

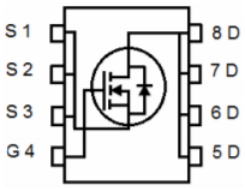
Features

- V_{DS}=30V, I_D=30A
  $R_{DS(ON)typ.}$ =9.0mΩ@VDS=10V
  $R_{DS(ON)typ.}$ =12.5mΩ@VDS=4.5V
- Fast switching
- High power and current handing capability
- Termination is Lead-free and RoHS Compliant

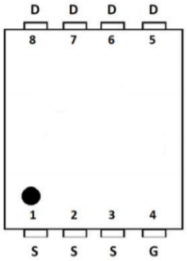
RoHS COMPLIANT

Applications

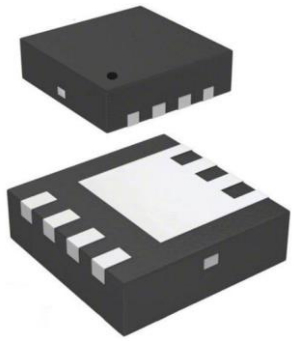
- PWM applications
- Load switch
- Power Management



Schematic Diagram



Pin Assignment



DFN3*3 Package

Maximum Ratings(T_A=25℃ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	I_D(T_C=25℃)	30	A
	I_D(T_C=100℃)	20	
Pulsed Drain Current[B]	I_{DM}	120	A
Maximum Power Dissipation[A]	P_D	9	W
Single pulse avalanche energy	E_{AS}	36	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance, Junction to Case	R_{QJA}	6.5	℃/W

Electrical Characteristics (T_A=25℃unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	30			V
Gate-Threshold Voltage	$V_{th(GS)}$	V_{DS}= V_{GS}, I_D=250 uA	1	1.5	2.2	V
Gate-body Leakage	IGSS	V_{DS}=0V, V_{GS}=±12V			±100	nA
Zero Gate Voltage Drain Current	IDSS	V_{DS}=30V, V_{GS}=0V			1	uA
Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5A		9	13	mΩ
		V_{GS} =4.5V, I_D =4A		12.5	17	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D =5A	10			s
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} =0V, F=1MHz		865		pF
Output Capacitance	C_{oss}			105		
Reverse Transfer Capacitance	C_{rss}			86		
Switching Capacitance						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}= 15V, R_L=3Ω V_{GS} = 10V, R_{GEN}=3Ω		5		nS
Turn-on Rise Time	t_r			4		nS
Turn-off Delay Time	$t_{d(off)}$			22		nS
Turn-off Fall Time	t_f			6		nS
Total Gate Charge	Q_g	V_{DS} = 15V, I_D=5A, V_{GS} =4.5V		18		nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS} =0V, I_D=5A			1.2	V
Diode Forward Current	Is				30	A

Notes:

A. The Power dissipation P_D is based on $T_{J(MAX)}$=150℃, using≤10s junction-to ambient thermal resistance.

B. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃.Ratings are based on low frequency and duty cycles to keep initial T_J=25℃.

C. The Static characteristics in Figures are obtained using 〈300 μs pulses, duty cycle 2% max.

D. EAS condition: TJ=25℃,V_{DD}=15V, V_{GS}=10V, R_G=25Ω, L=0.5Mh, I_{AS}=19A。

Typical Electrical and Thermal Characteristics

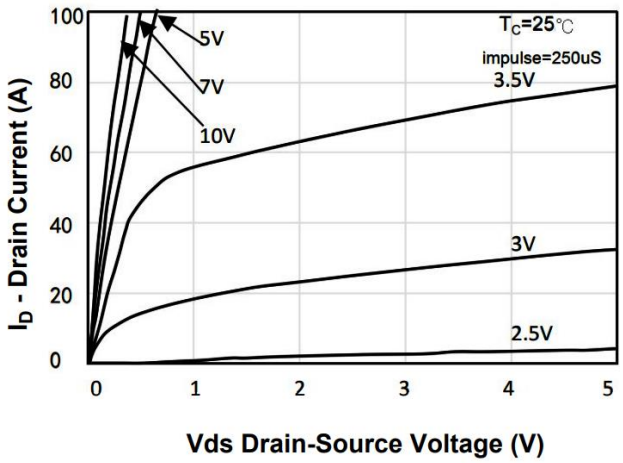


Figure 1. On-Region Characteristics

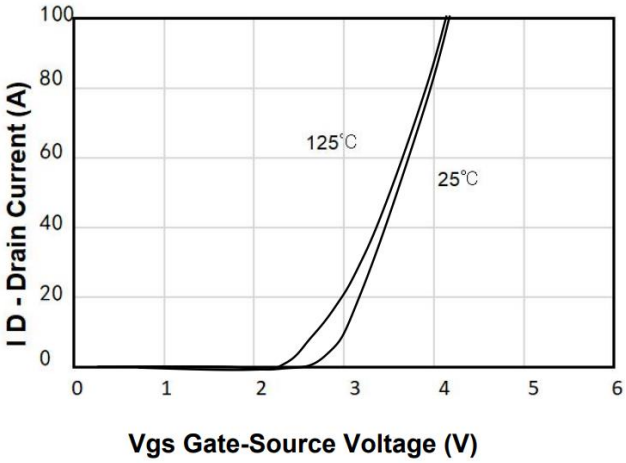


Figure 2. Transfer Characteristics

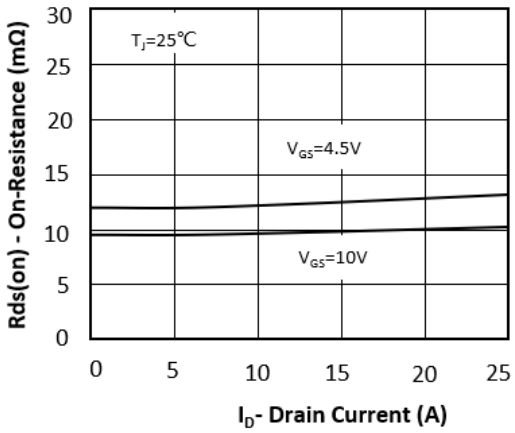


Figure 3. On-resistance vs. Drain Current

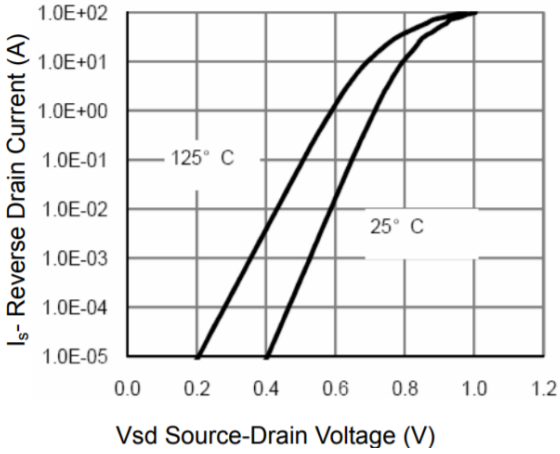


Figure 4. Body Diode Characteristics

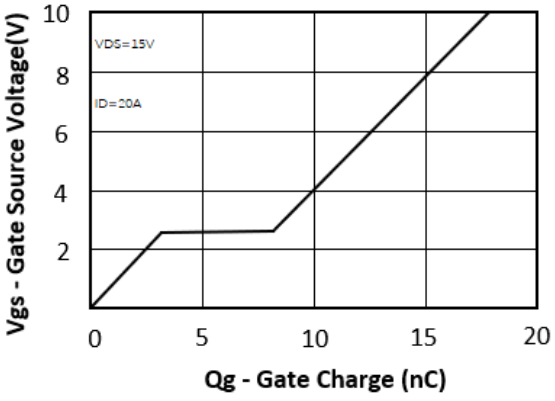


Figure 5. Gate Charge Characteristics

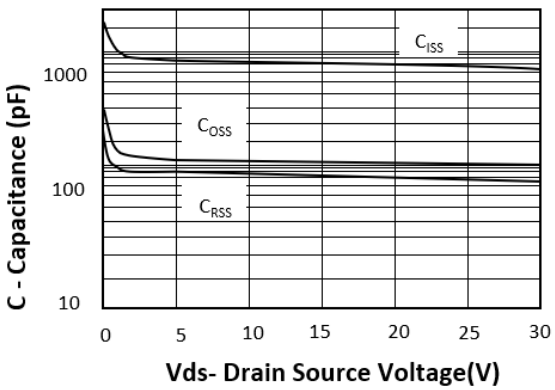


Figure 6. Capacitance Characteristics

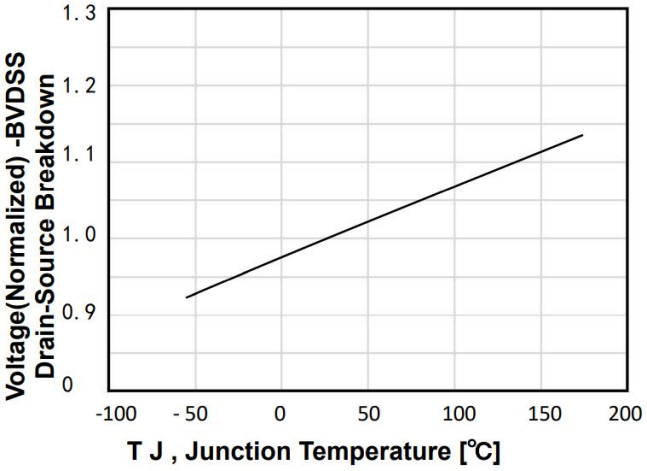


Figure 7. Breakdown Voltage Variation vs Temperature

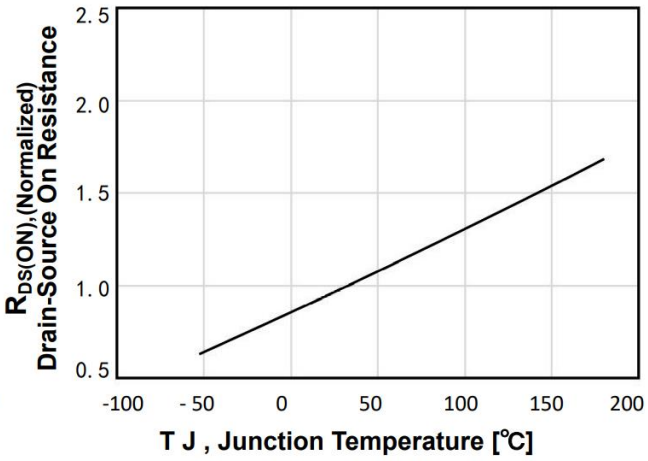


Figure 8. On-Resistance Variation vs Temperature

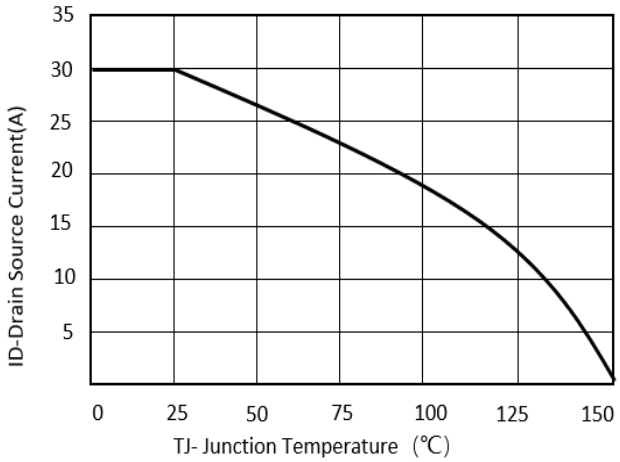


Figure 9. Current – Junction Temperature

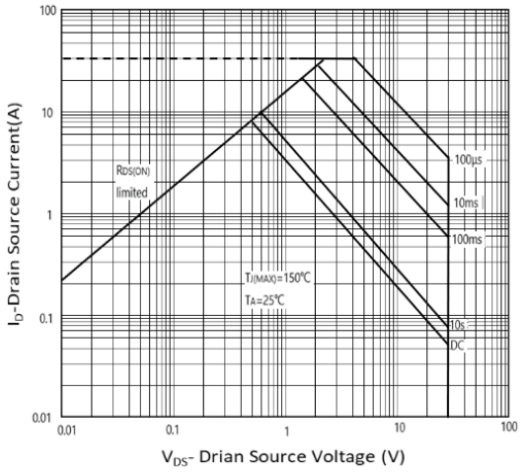


Figure 10. Safe Operation Area

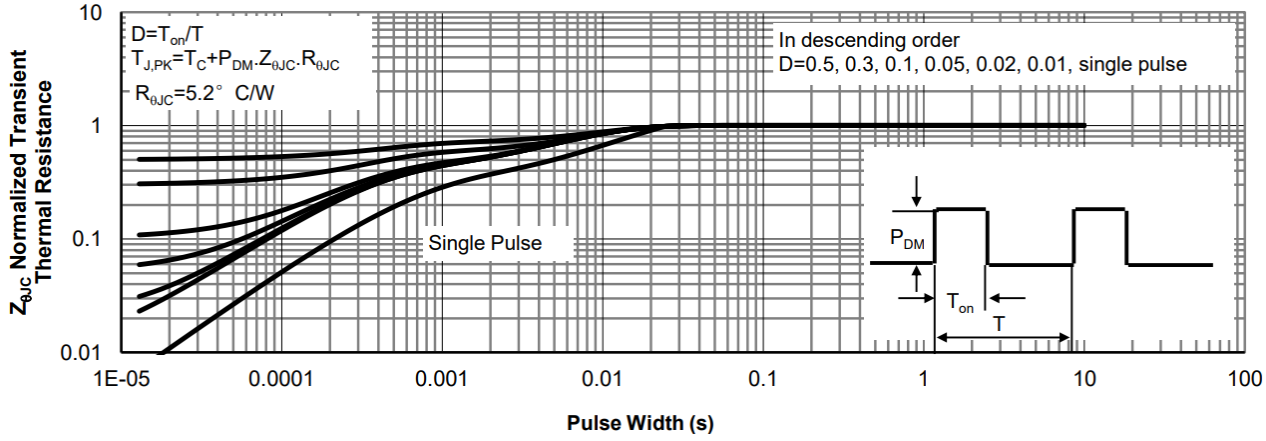
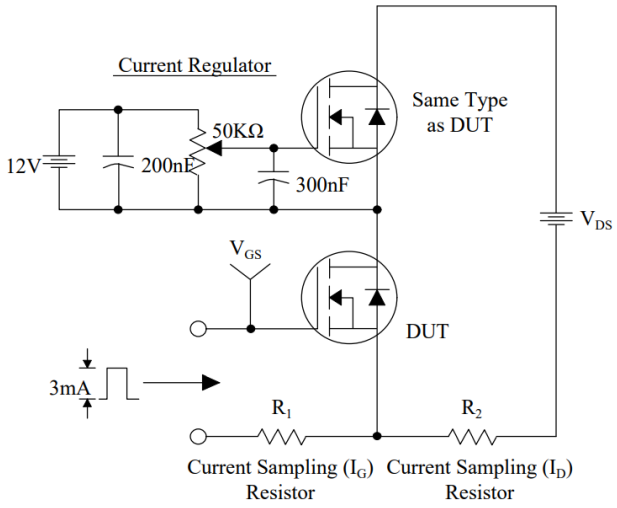
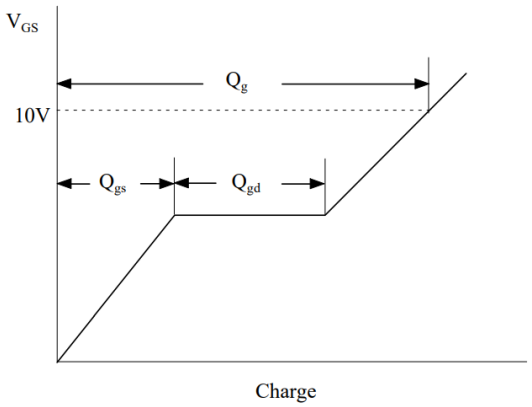


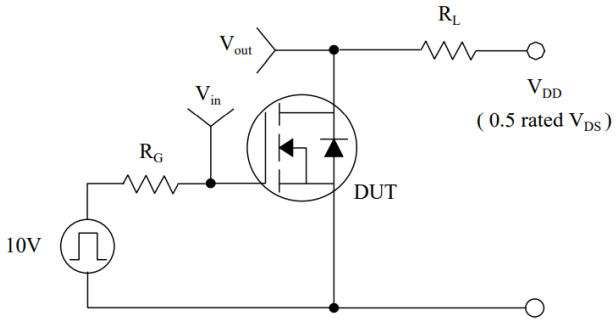
Figure 11. Normalized Maximum Transient Thermal Impedance

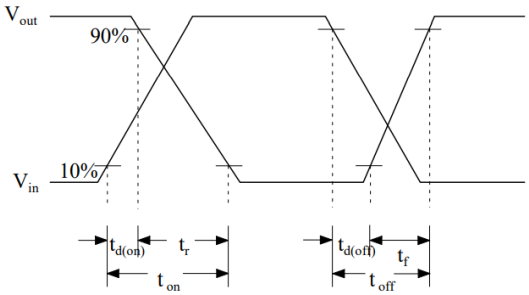
Gate Charge Test Circuit & Waveform



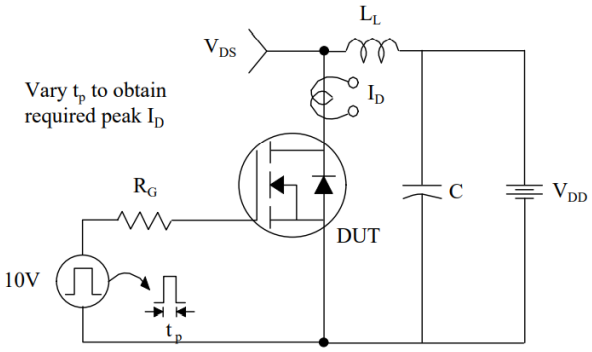


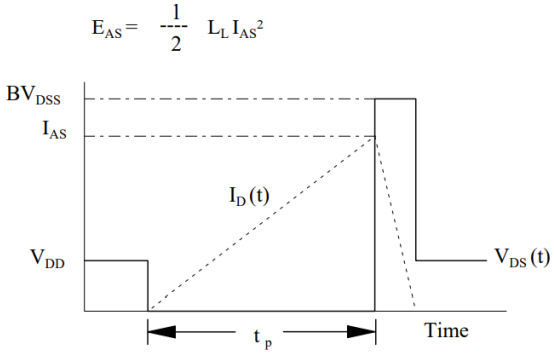
Resistive Switching Test Circuit & Waveforms



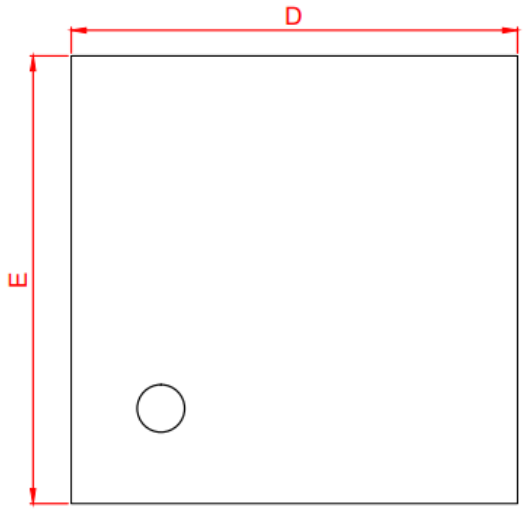


Unclamped Inductive Switching Test Circuit & Waveforms

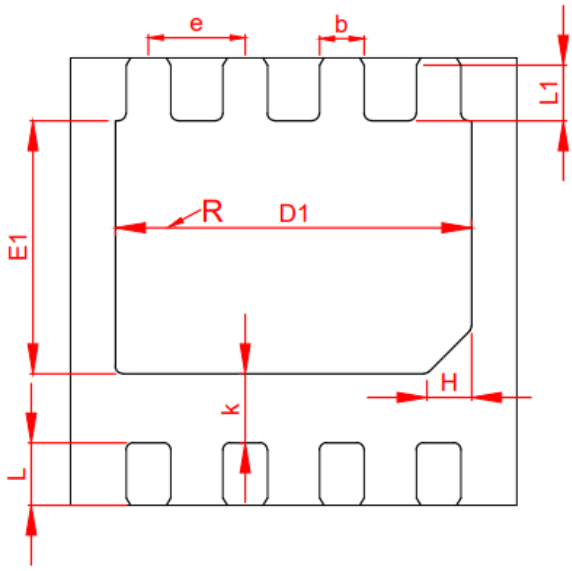




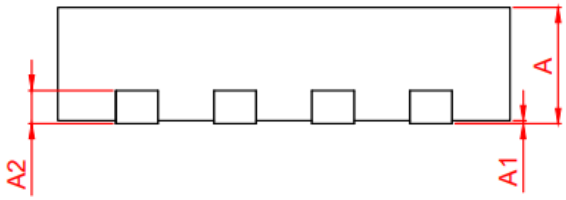
DFN3*3 Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
* A1	0.00	0.02	0.05
* b	0.27	0.32	0.37
* A2	0.20REF		
* D	2.90	3.00	3.10
* E	2.90	3.00	3.10
* E1	1.70	1.80	1.90
* D1	2.35	2.45	2.55
* e	0.65BSC		
* L	0.35	0.40	0.45
h	0.30 REF		
* k	0.50REF		
* L1	0.25	0.30	0.35

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